

MODEL NAME : BAP10(15")/BAP20(17")  
PROJECT CODE : ANRBAP1000/ANRBAP2000  
PCB NO :  
DAB0001H000 LA-D752P M/B(AMD)  
DA4002AV000 LS-D751P LOGO\_15/B  
DA80017I000 LS-D752P LOGO\_17/B  
DA4002B000S LS-D753P PWR\_15/B  
DA4002AW000 LS-D754P PWR\_17/B  
DA80017J000 LS-D755P IO\_12L/B  
DA4002B100S LS-D756P SSD/B  
DA4002AY000 LS-D757P TRON\_TOP/B \*2  
DA4002AZ000 LS-D758P TRON\_BOT/B \*4  
DA80017K000 LS-D759P IO\_14L/B  
DA30000W300 LF-D751P Head\_15/B  
DA30000W400 LF-D752P Head\_17/B  
DA30000SY00 LF-D753P TRON/B \*2

ZZZ PCB@  
PCB 1QB LA-D752P REV0 MB AMD 10  
DAB0001H000

ZZZ PCBR1@  
PCB 1FU LA-C901P REV1 M/B MLK 3  
DAA000AK010

ZZZ PCBR3@  
PCB 1FU LA-C901P REV1 MB MLK TRIP 3 A31!  
DAA000AK011

ZZZ DAZR1@  
PCB AAP01 LA-C901P LS-A302P/A303P/C904P 02  
DAZ1FU00100

ZZZ DAZR3@  
PCB AAP01 LA-C901P LS-A302P/A303P/C904P 02 TRIPOD A31 !  
DAZ1FU00101

HDMI@	ROYALTY HDMI W/LOGO
Part Number	Description
R0000000020M	HDMI W/Logo:R0000000020M

Layout Dell logo



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REV: X00  
PWB: XXXXX  
DATE: 1450-06

Cassini 15/17" Skylake/Kabylake-H 45W

Skylake/Kabylake PCH with AMD E-class R16M

REV : 0.1 (X00)

2016.01.22

@ : Nopop Component

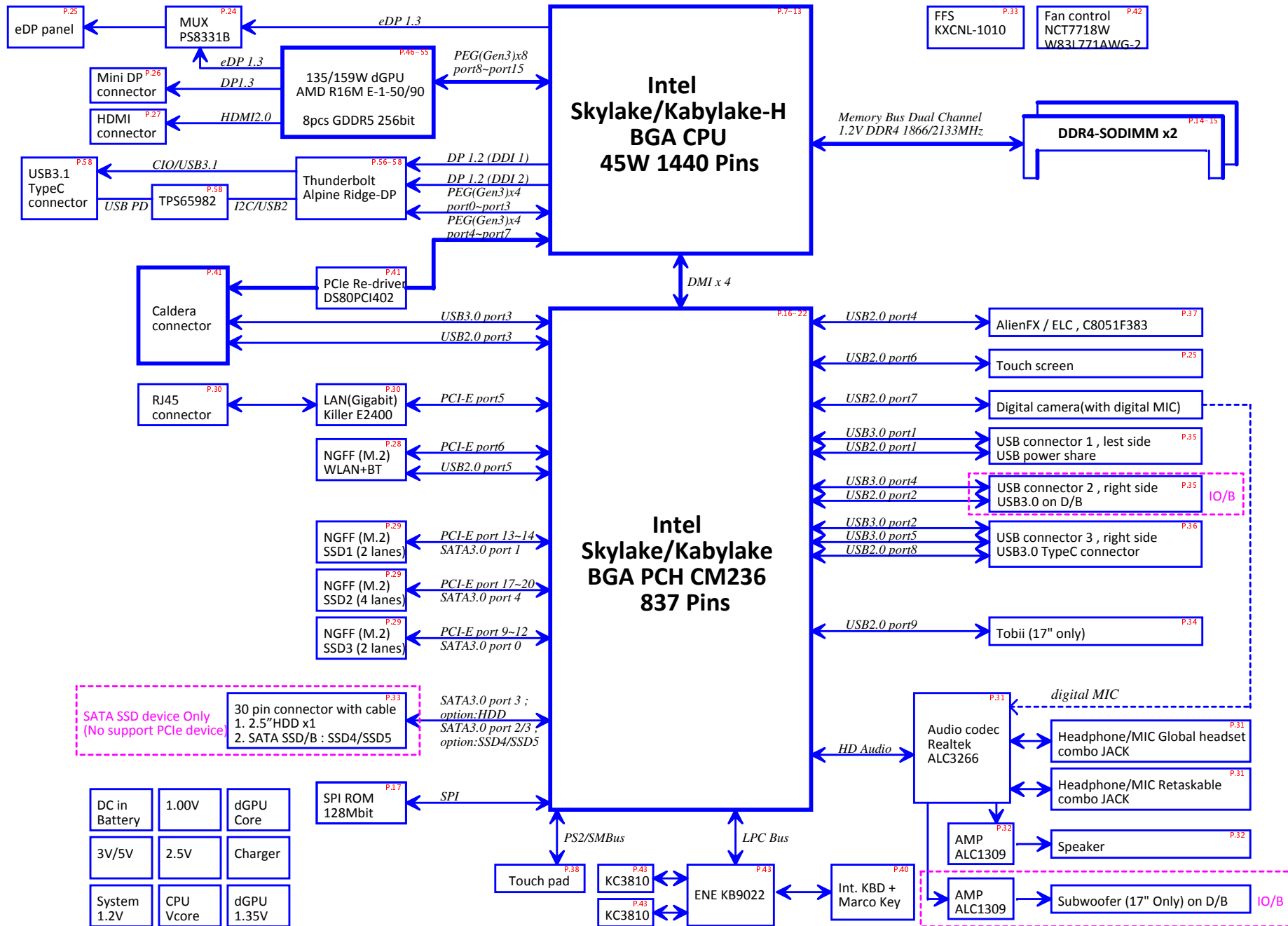
EMI@,ESD@,RF@ : EMI/ESD/RF part

CONN@ : Connector Component

@EMI@,@ESD@,@RF@ : Total debug Component

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				Date	Thursday, January 21, 2016
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				Rev	0.1

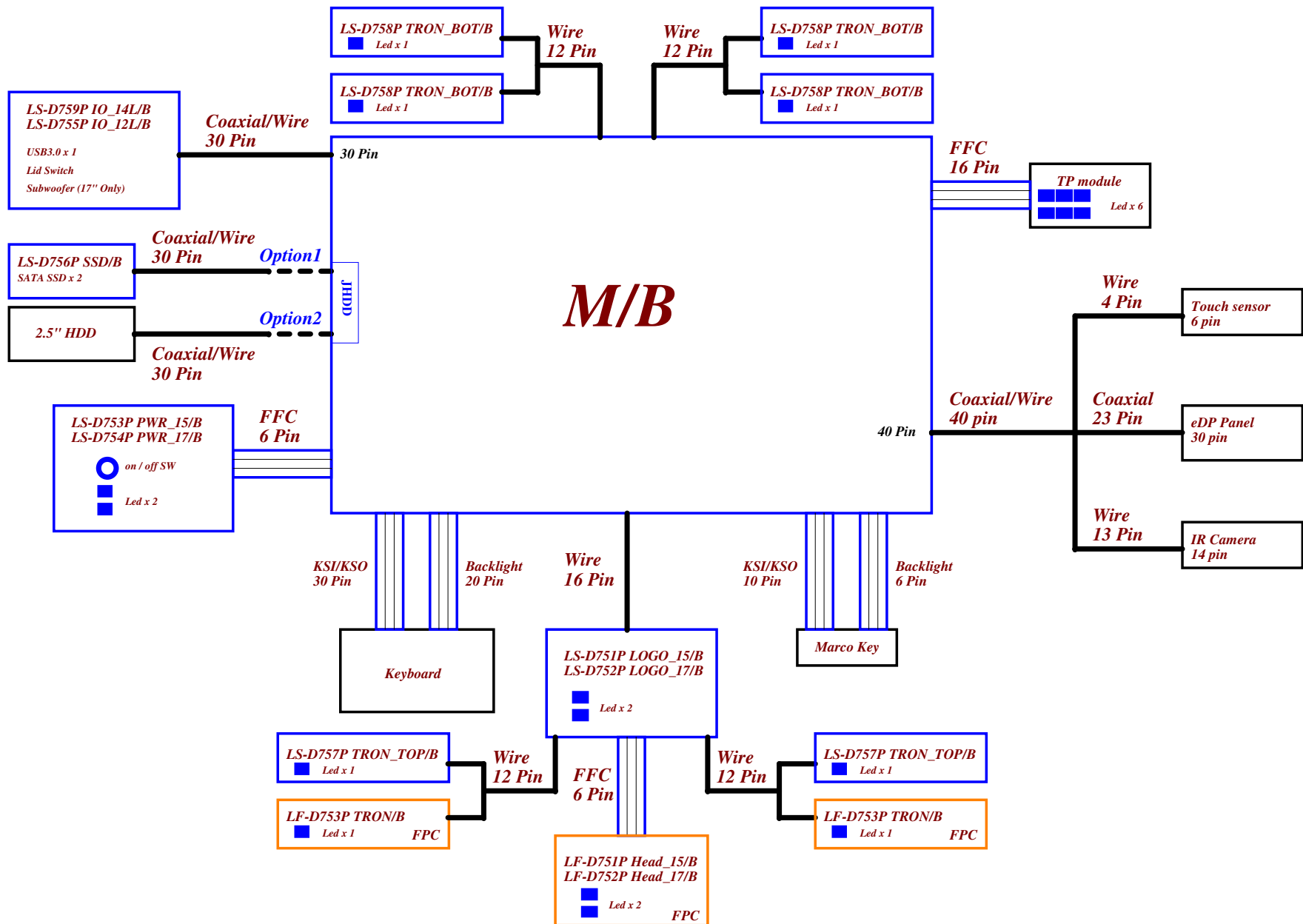
# Block Diagram



PCB

FPC

Module



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Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF

Voltage Rails

Power Plane	Description	S0	S3	S4 / S5
VIN	Adapter power supply	N/A	N/A	N/A
BATT+	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF
+1VALW	System +1VALW power rail	ON	ON	ON*
+1V_PRIM	System +1VALW power rail	ON	ON	ON*
+VCCIO	+1.0VS IO power rail	ON	OFF	OFF
+VGA_PCIE	+1.0VS power rail for GPU	ON	OFF	OFF
+MEM_GFX	+1.5VS power rail for GPU	ON	OFF	OFF
+1.2V_VDDQ	DDR-IV +1.2V power rail	ON	ON	OFF
+1VS_VCCST	+1.0V power rail for CPU	ON	ON	OFF
+1VS_VCCSTG	+1.0VS power rail for CPU	ON	OFF	OFF
+3VALW	System +3VALW always on power rail	ON	ON	ON*
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON*
+3V_LAN	+3VALW power for LAN power rails	ON	ON	ON*
+3VS	System +3VS power rail	ON	OFF	OFF
+1.8VS	+1.8VS power rail for GPU	ON	OFF	OFF
+3VGS	+3VS power rail for GPU	ON	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON*
+5VS	System +5VS power rail	ON	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON
+VCC_SA	System Agent power rail	ON	OFF	OFF

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF

Board ID TABLE

ID	PCB Revision
NV	AMD
0	10
1	11
2	12
3	13
4	14
5	15

PCH-H CM236

HSIO	USB3	PCIe	SATA3	Function
1	1			JUSB1,type A
2	2			JUSBC2,type C
3	3			Caldera
4	4			JIO,IO/B
5	5			JUSBC2,type C
6	6			
7	7	1		
8	8	2		
9	9	3		
10	10	4		
11		5		LAN
12		6		WLAN
13		7		
14		8		
15		9	0	JSSD3
16		10	1	M.2 2280
17		11		SATA
18		12		PCIe x4(When SSD/B exist)
22		16	3	JSSD5/HDD SATA
21		15	2	JSSD4 SATA
20		14	1	JSSD1
19		13	0	SATA/PCIe x2
23		17	4	JSSD2
24		18	5	M.2 2280
25		19		SATA
26		20		PCIe x4

\* PCIe 13~16 in "Lane Reversal Mode". (HSIO Port 19~22)

USB2	Function
1	JUSB1(Powershare)
2	JIO(IO/B)
3	Caldera
4	ELC
5	Bluetooth
6	Touch screen
7	Camera
8	JUSBC2
9	Tobii
10	
11	
12	
13	
14	

Symbol Note :



Digital Ground



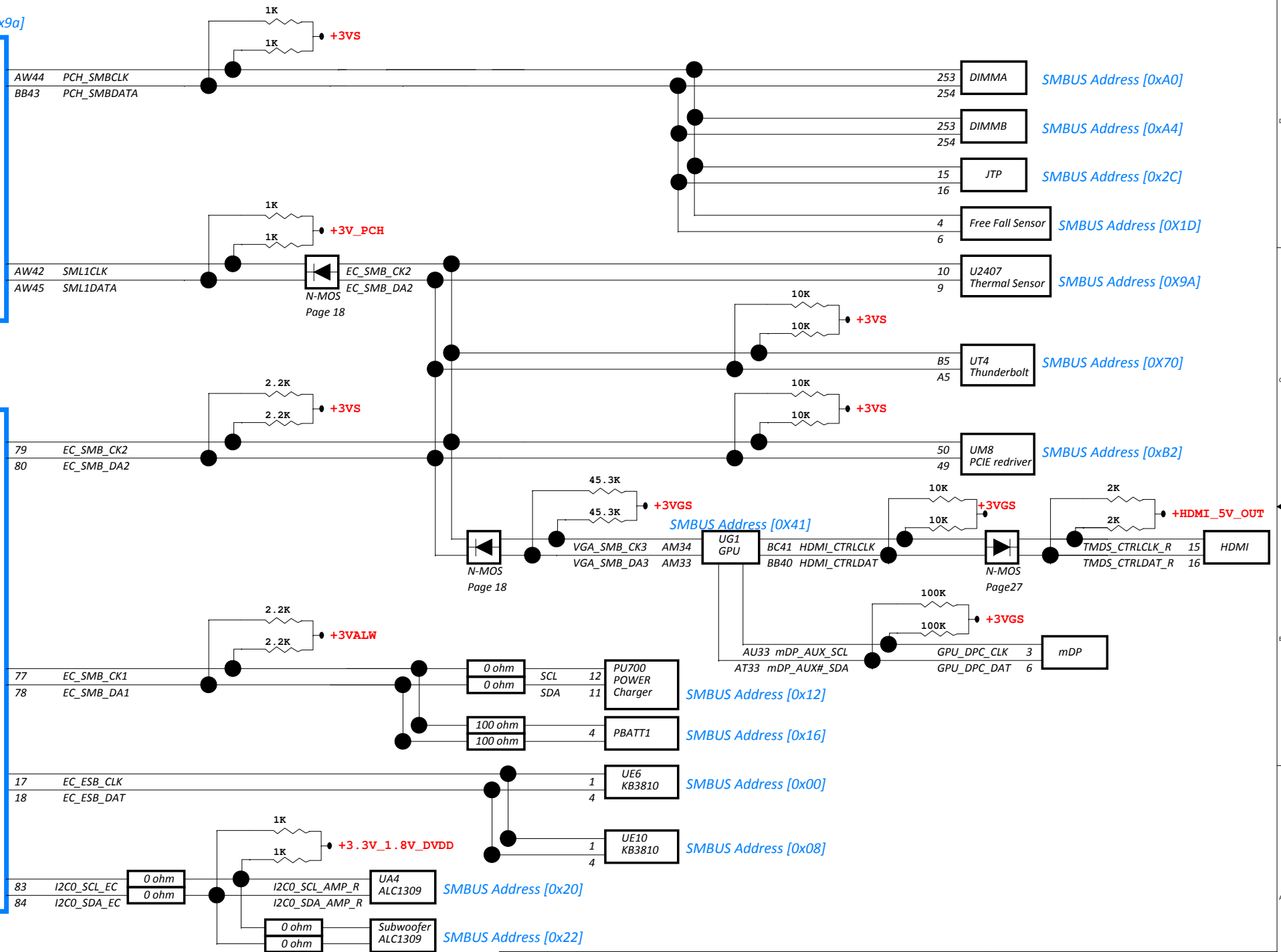
Analog Ground

CPU,C  
DDR,D  
GPU,DP,HDMI,EDP,V  
LAN,L  
AUDIO,A  
NGFF,N  
USB,U  
CALDERA,M  
HDD,S  
ELC,E  
FAN,F  
TP,T  
KBC,K  
DC,O

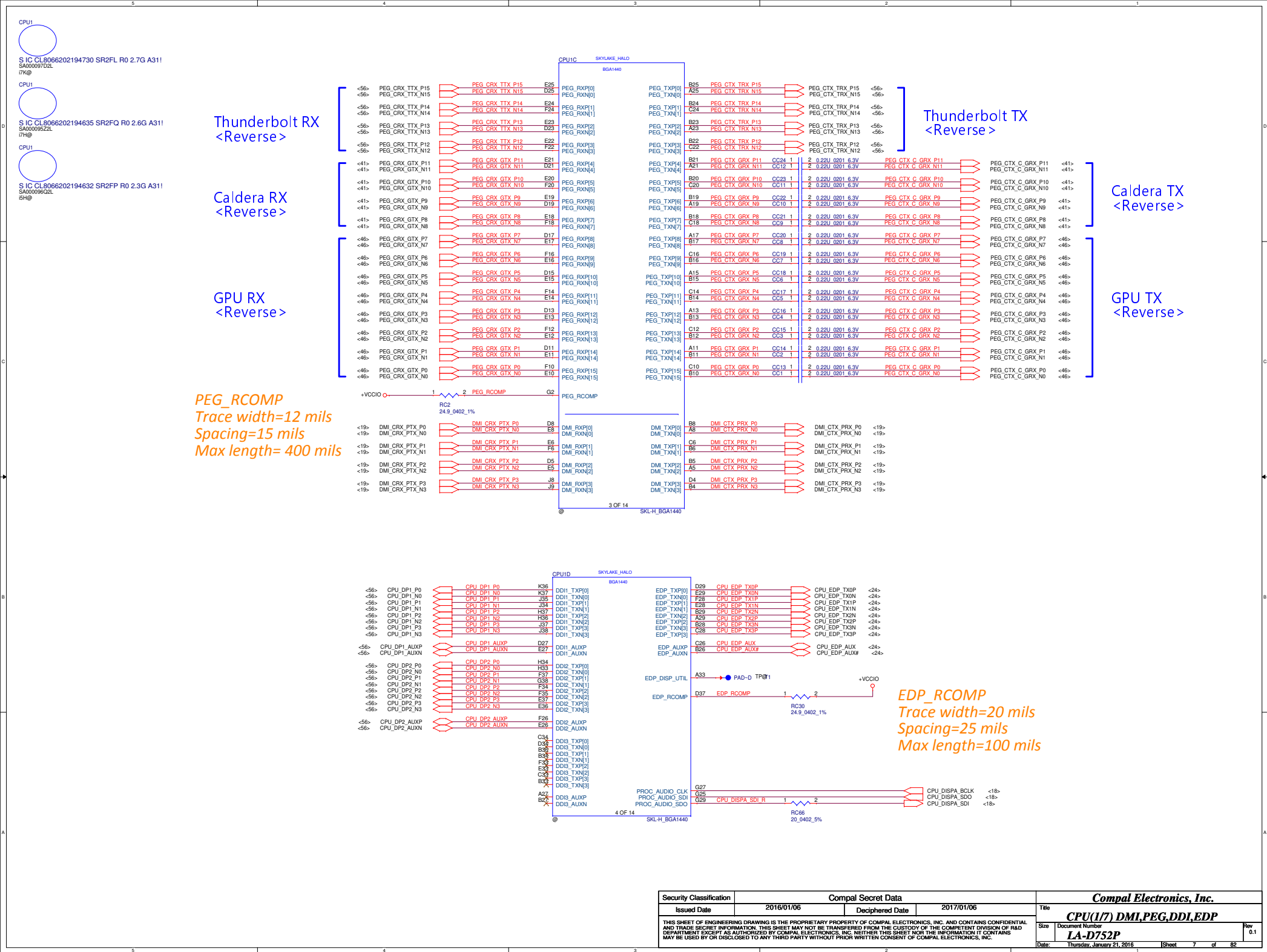
SMBUS Address [0x9a]

Kaby lake  
PCH-H

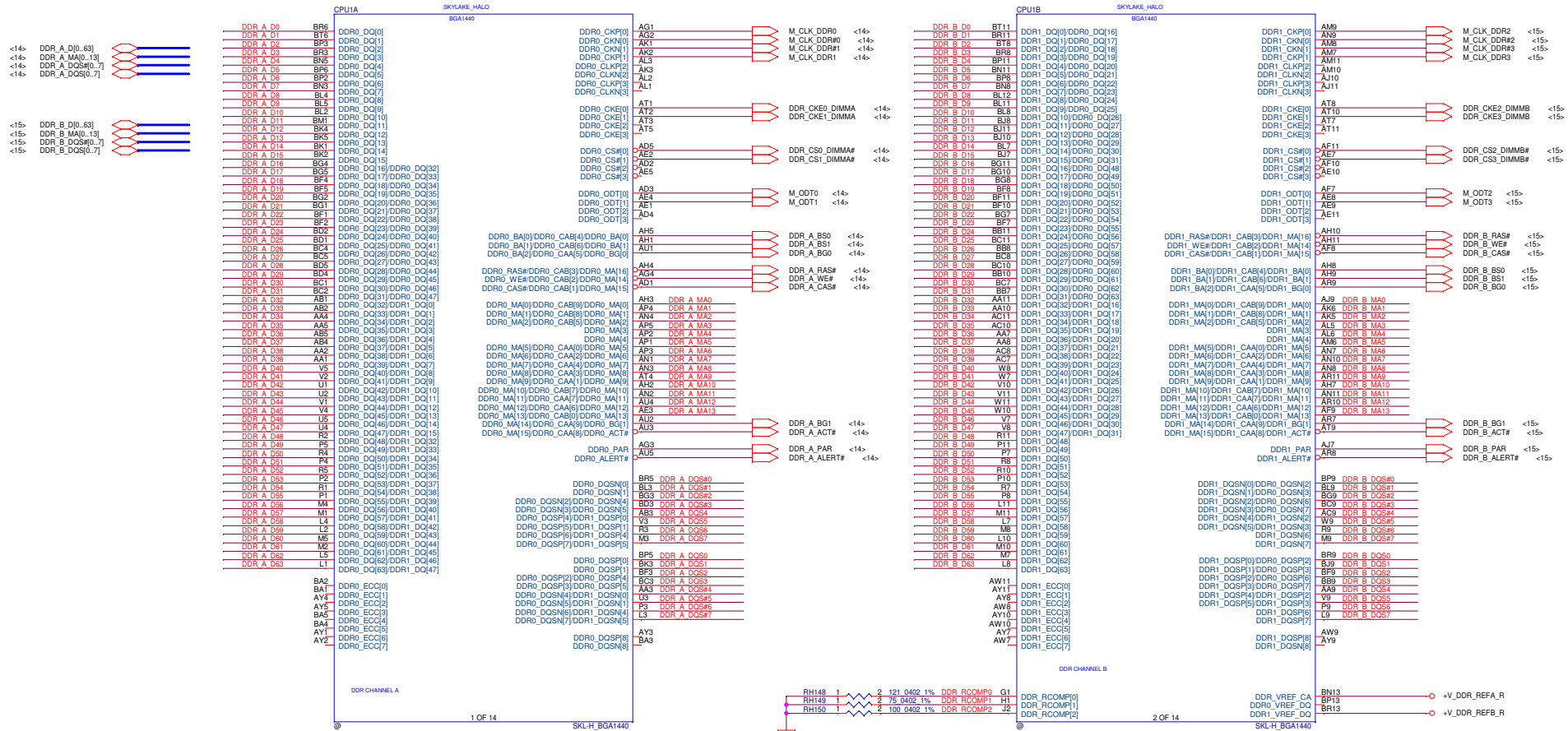
KBC  
KB9022QD







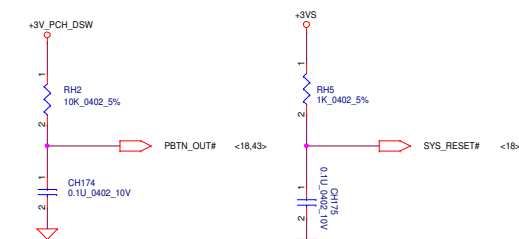
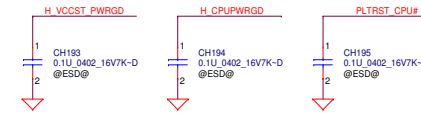
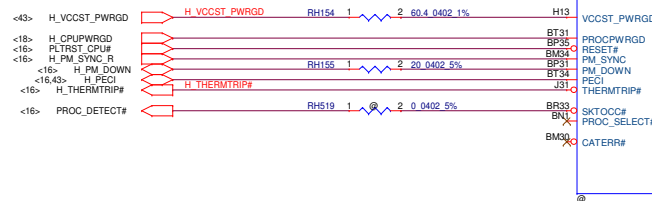
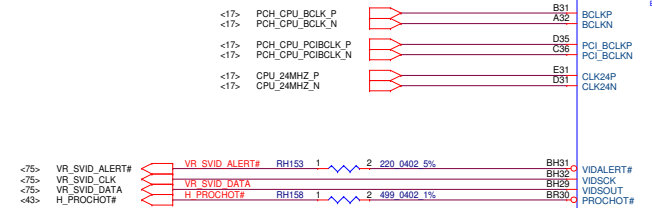
## Interleave

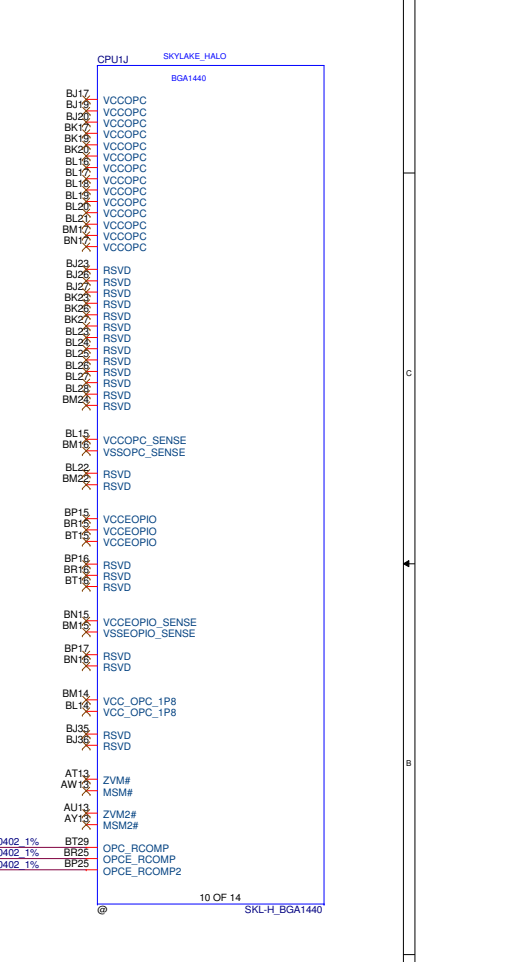
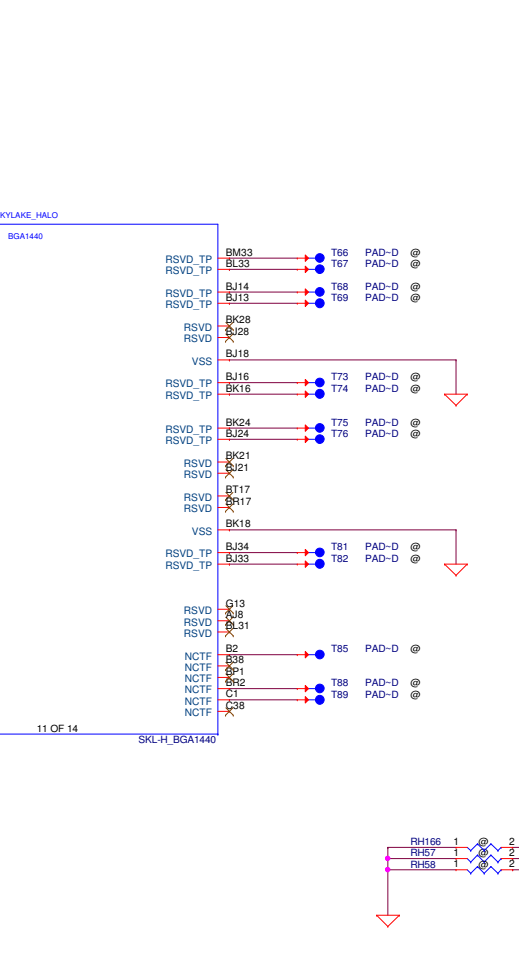
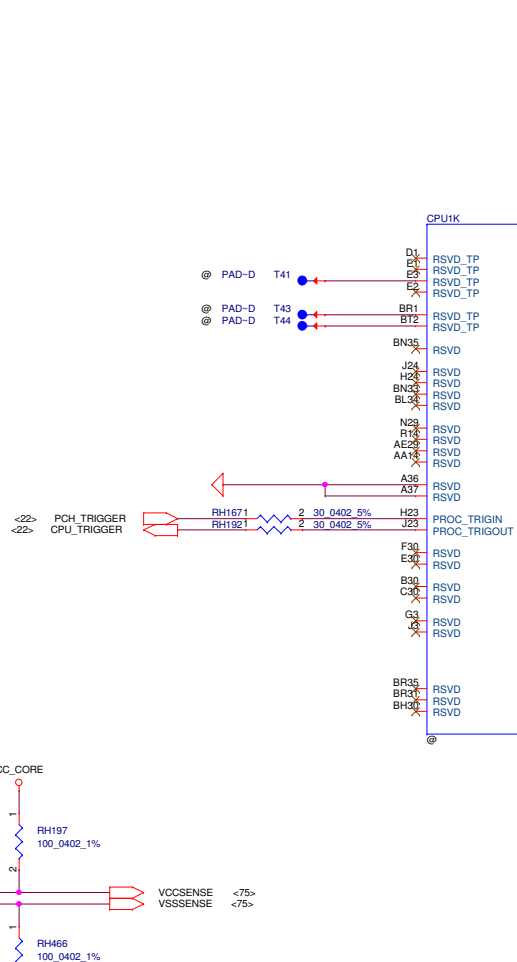
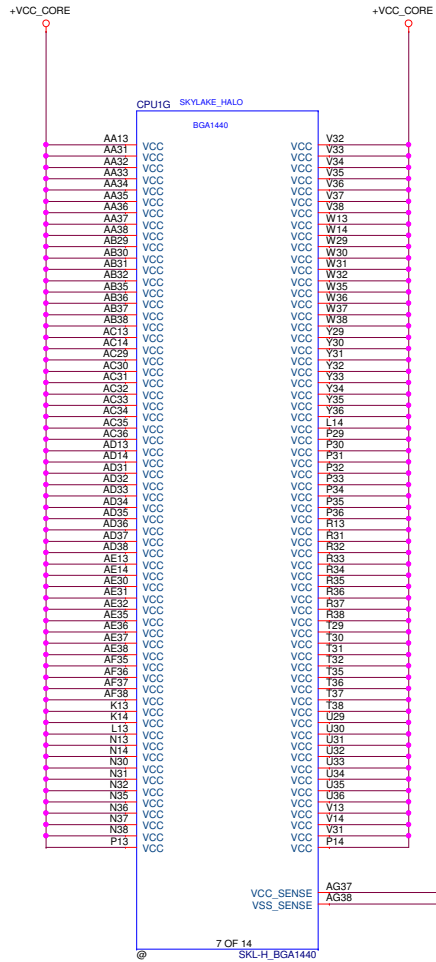


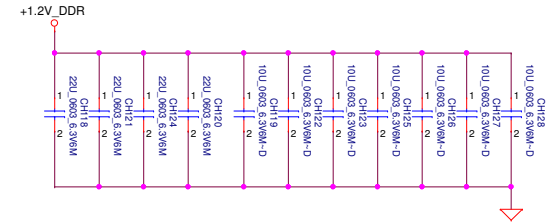
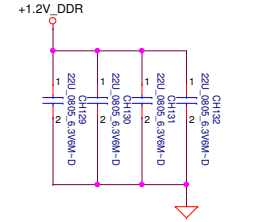
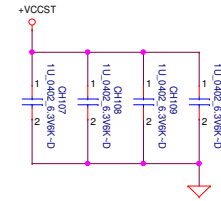
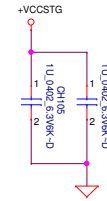
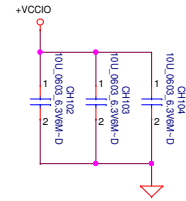
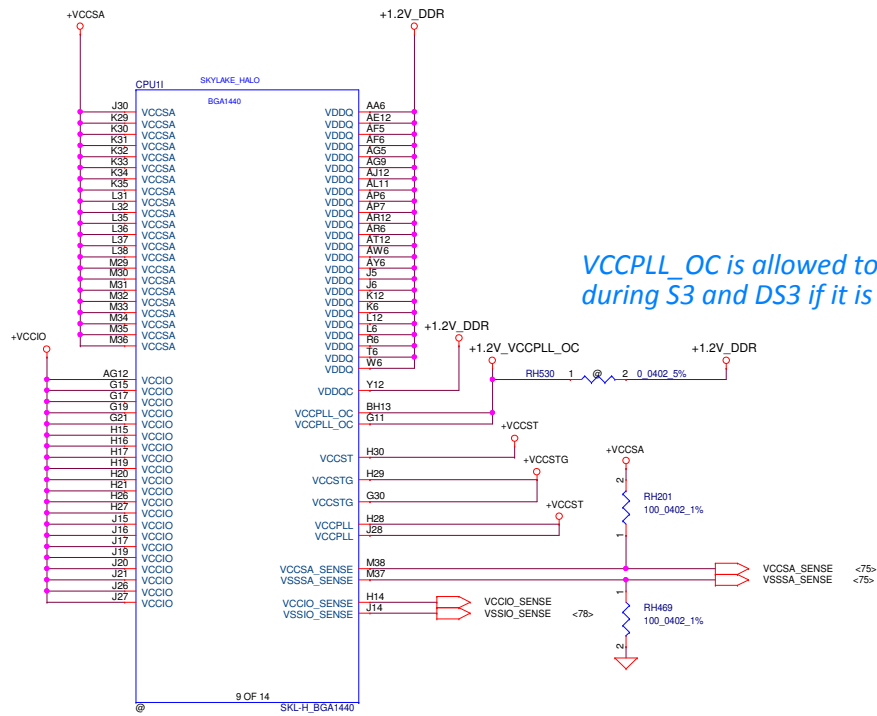
DDR\_RCOMP0 :  
DDR\_RCOMP1 :  
DDR\_RCOMP2 :  
Trace width=12~15 mils  
Spacing=20 mils  
Max length= 500 mils

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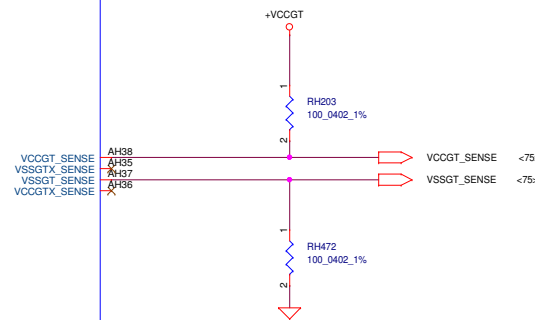
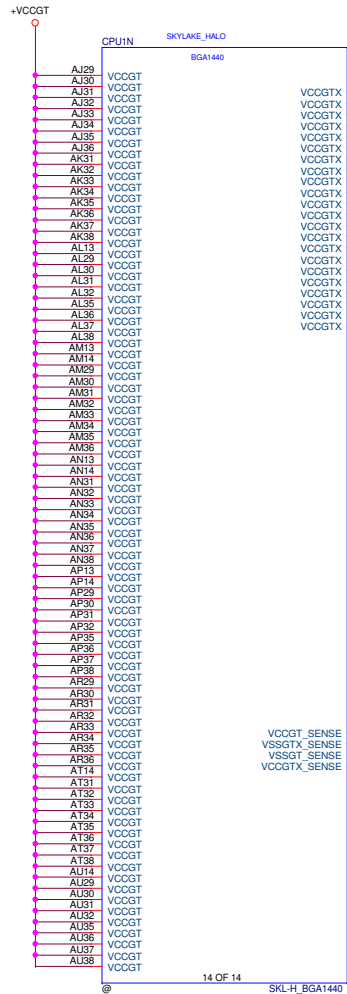
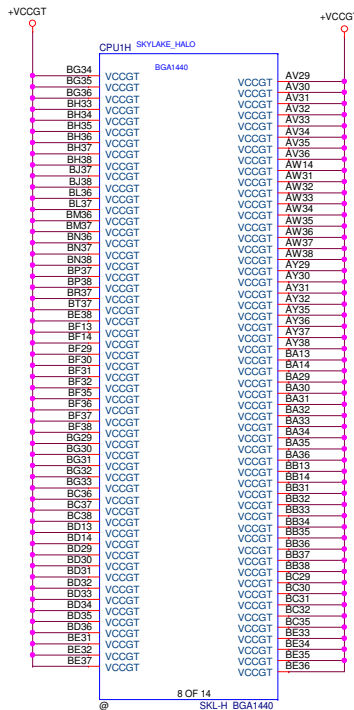




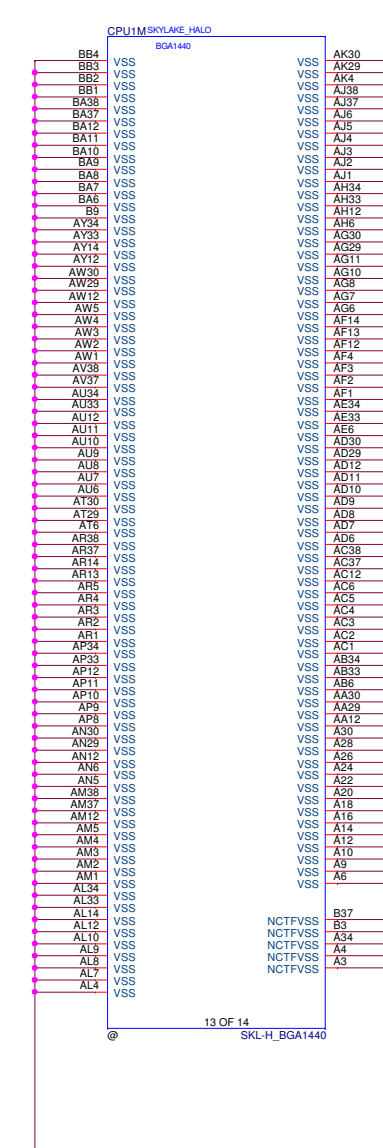
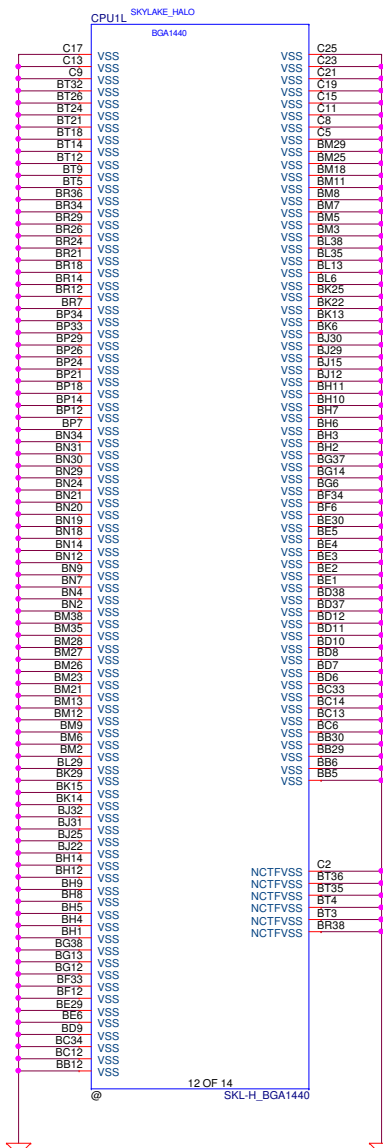
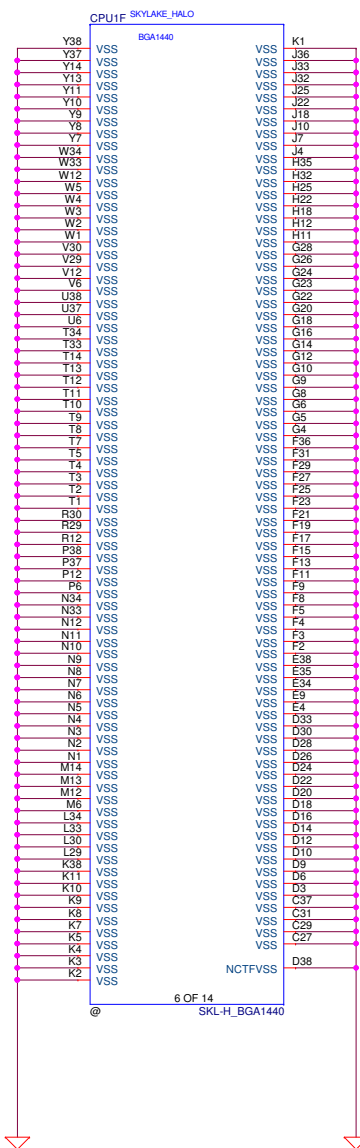




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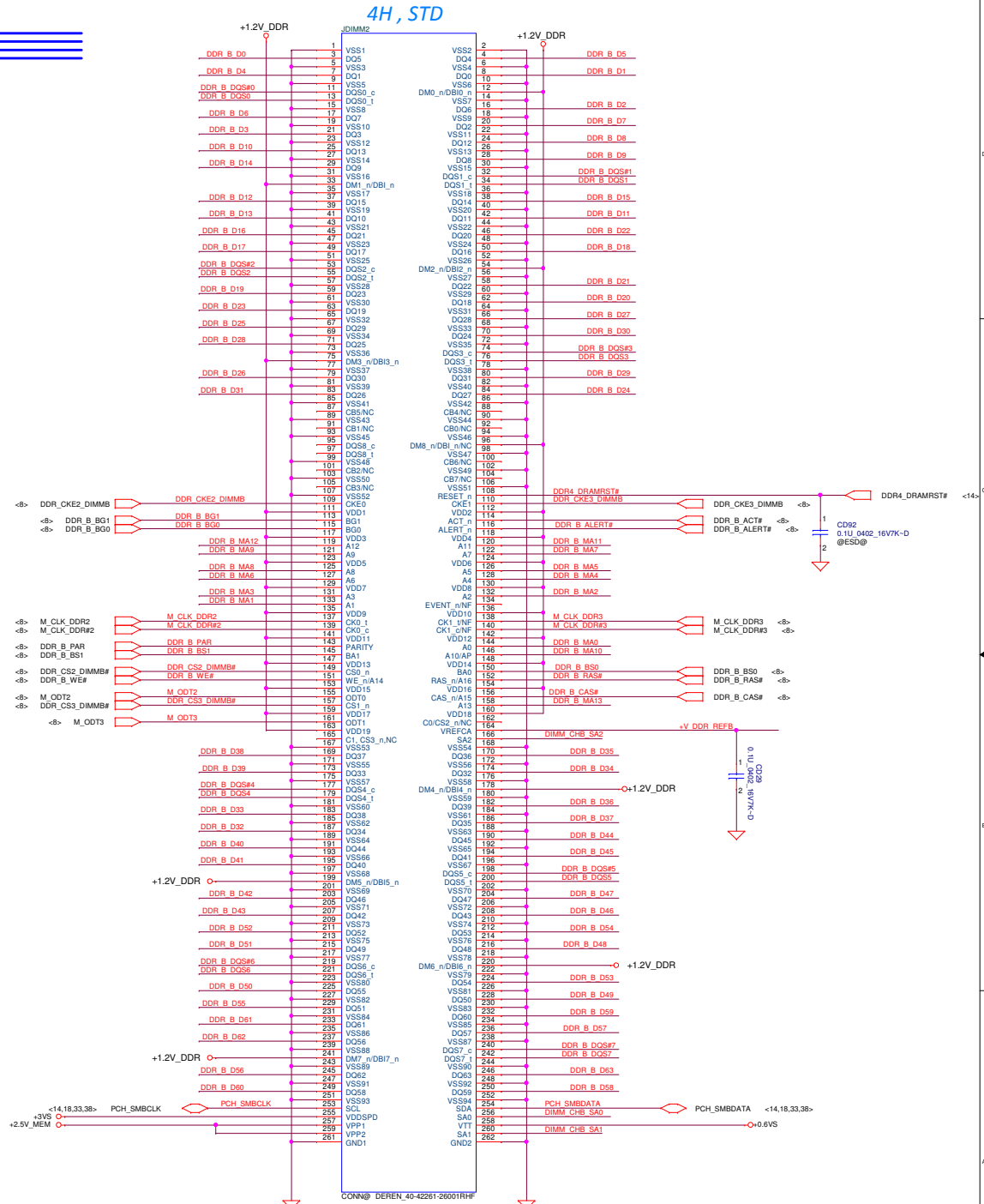
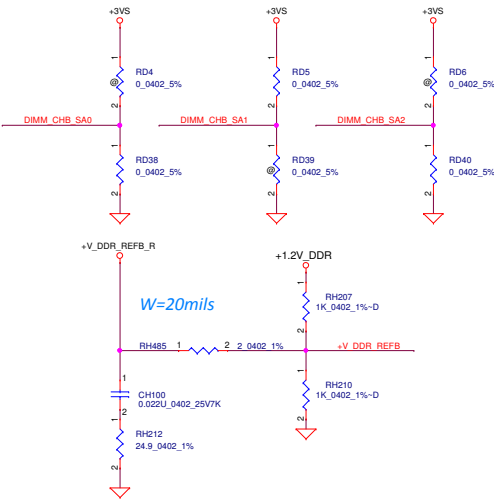
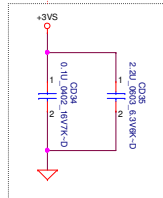
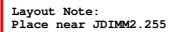
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>CPU(7/7) VSS</b>	
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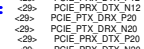
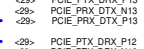
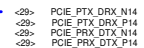
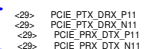
The diagram shows a 5V regulator circuit. The input is labeled +2.5V\_MEM. The feedback network consists of a 100k resistor (labeled 100 0000 6.316M-D) and a 100nF capacitor (labeled C030 100 0000 6.316M-D) connected in parallel between the output and the inverting input. The output is connected to a load, represented by a triangle symbol.

The top diagram shows a 1.2V DDR module connected to a processor pin header. The module's internal components, including capacitors and resistors, are shown. The connection to the processor's pins is indicated by a red triangle.

The bottom diagram shows a 1.2V DDR module connected to a processor pin header. The module's internal components, including capacitors and resistors, are shown. The connection to the processor's pins is indicated by a red triangle.

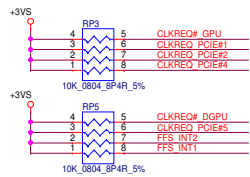


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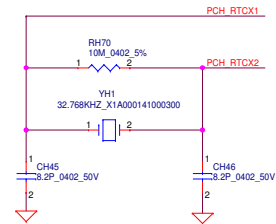


<b>Compal Electronics, Inc.</b>			
Title		<b>PCH (1/7) SATA,DDC,PCIE</b>	
Size	Document Number	Rev	
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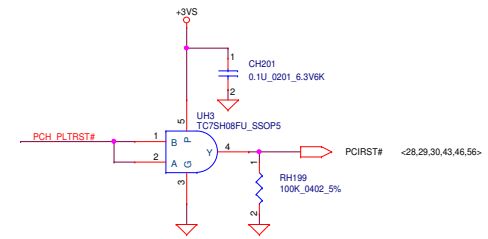
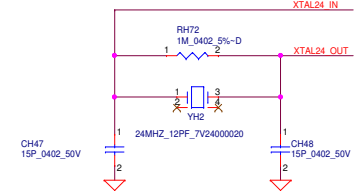




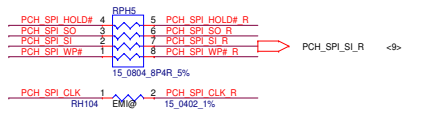
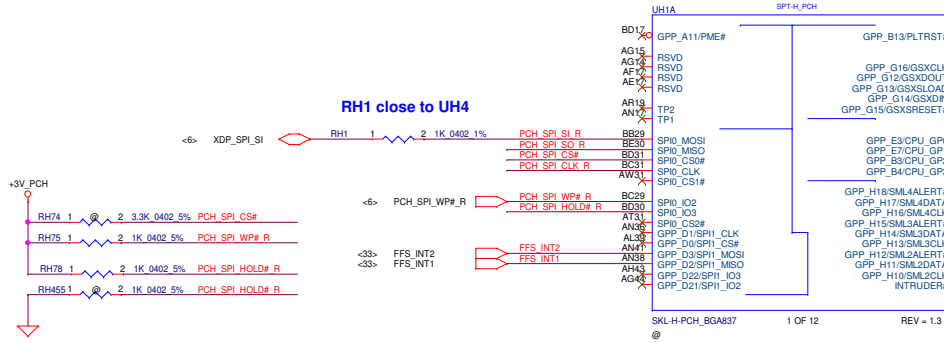
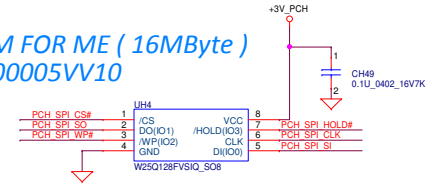
- 0. PEG
- 1. SSD1
- 2. SSD2
- 3. TBT
- 4. LAN
- 5. WLAN
- 6. Caldera
- 7. SSD3



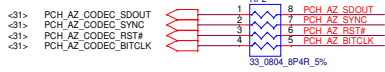
RTC CRYSTAL  
Max Crystal ESR  
= 50k Ohm.



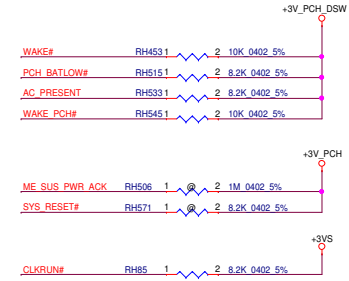
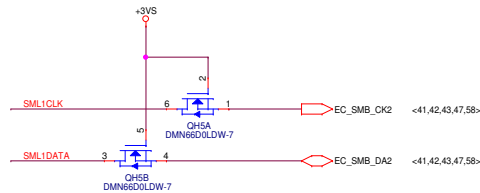
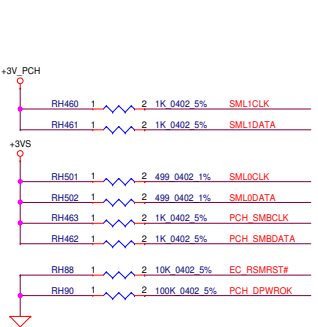
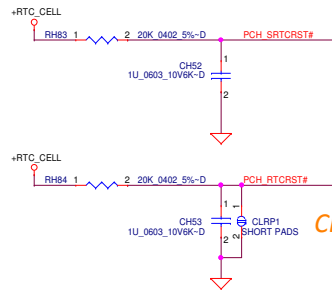
SPI ROM FOR ME ( 16MByte )  
PN: SA00005VV10



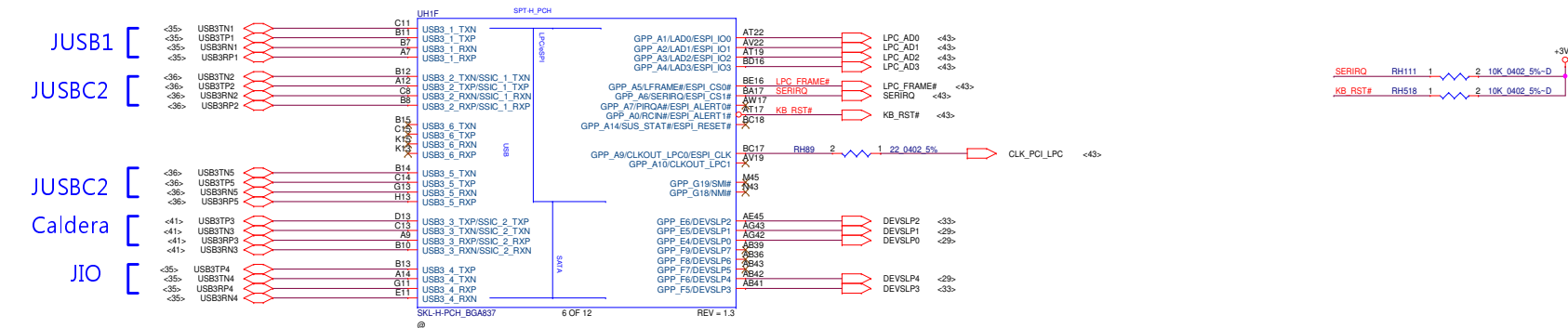
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title
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				Size Document Number
				LA-D752P
				Date: Thursday, January 21, 2016
				Sheet 17 of 82



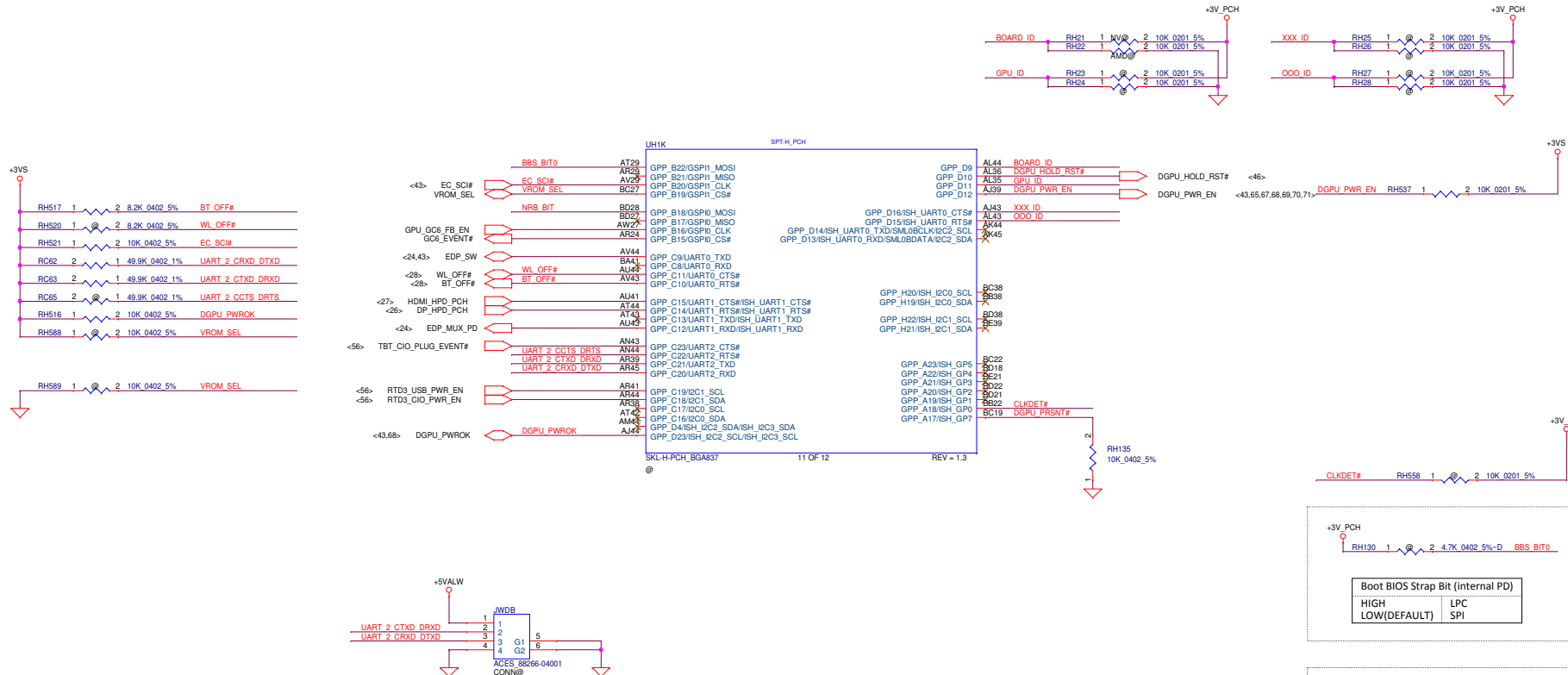
## PCH to DDR, XDP, FFS

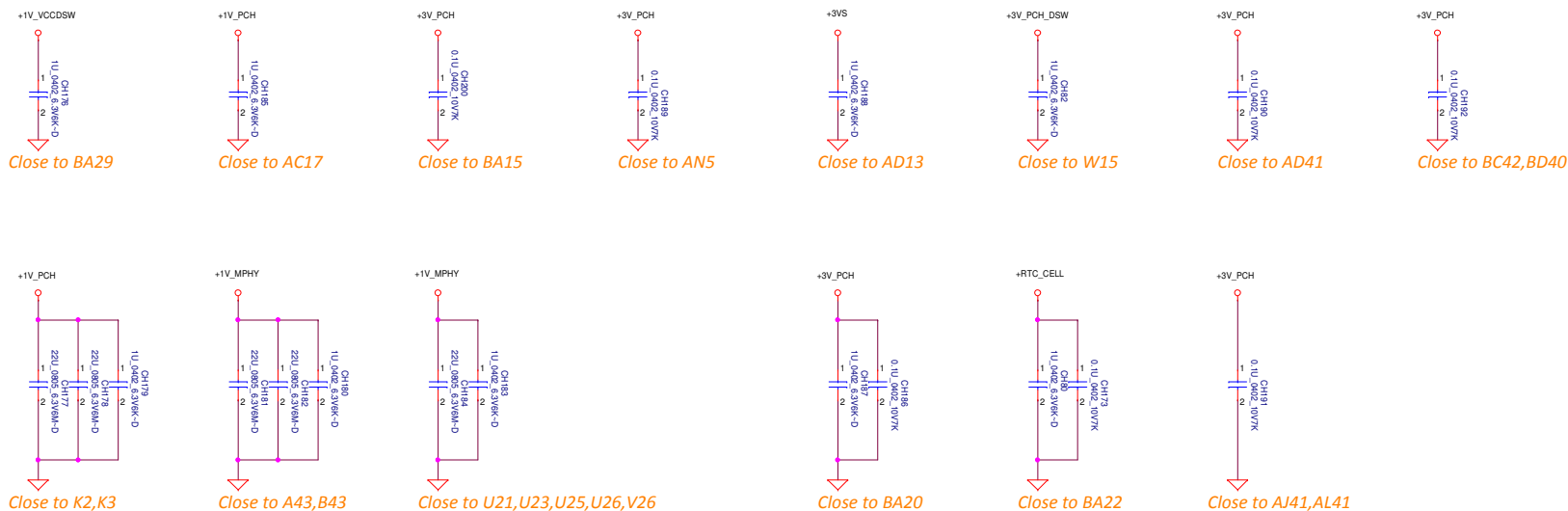


Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title
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				Size Document Number
				LA-D752P
				Date: Thursday, January 21, 2016
				Sheet 18 of 82

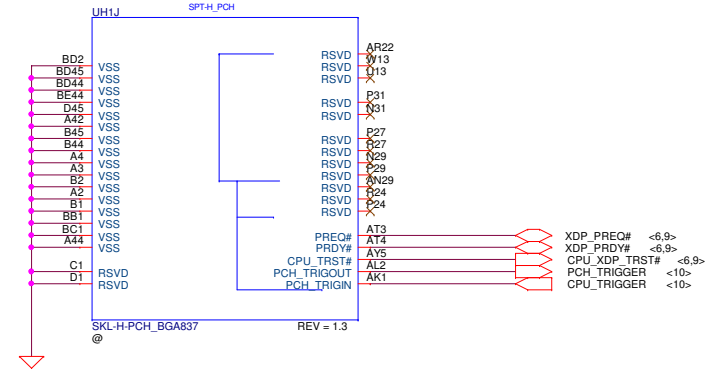
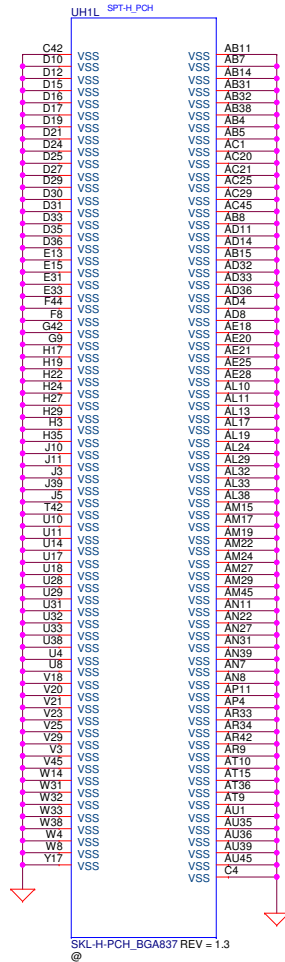
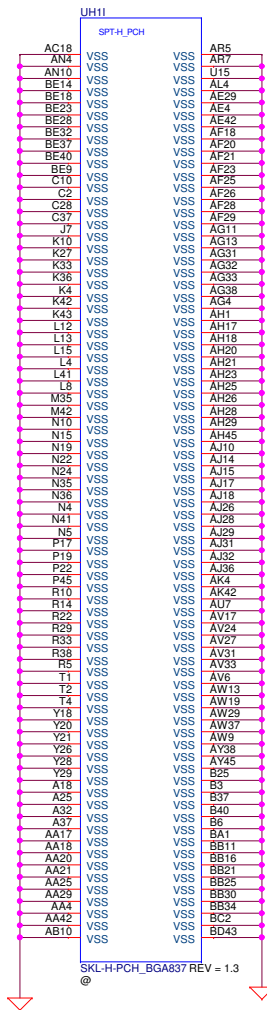


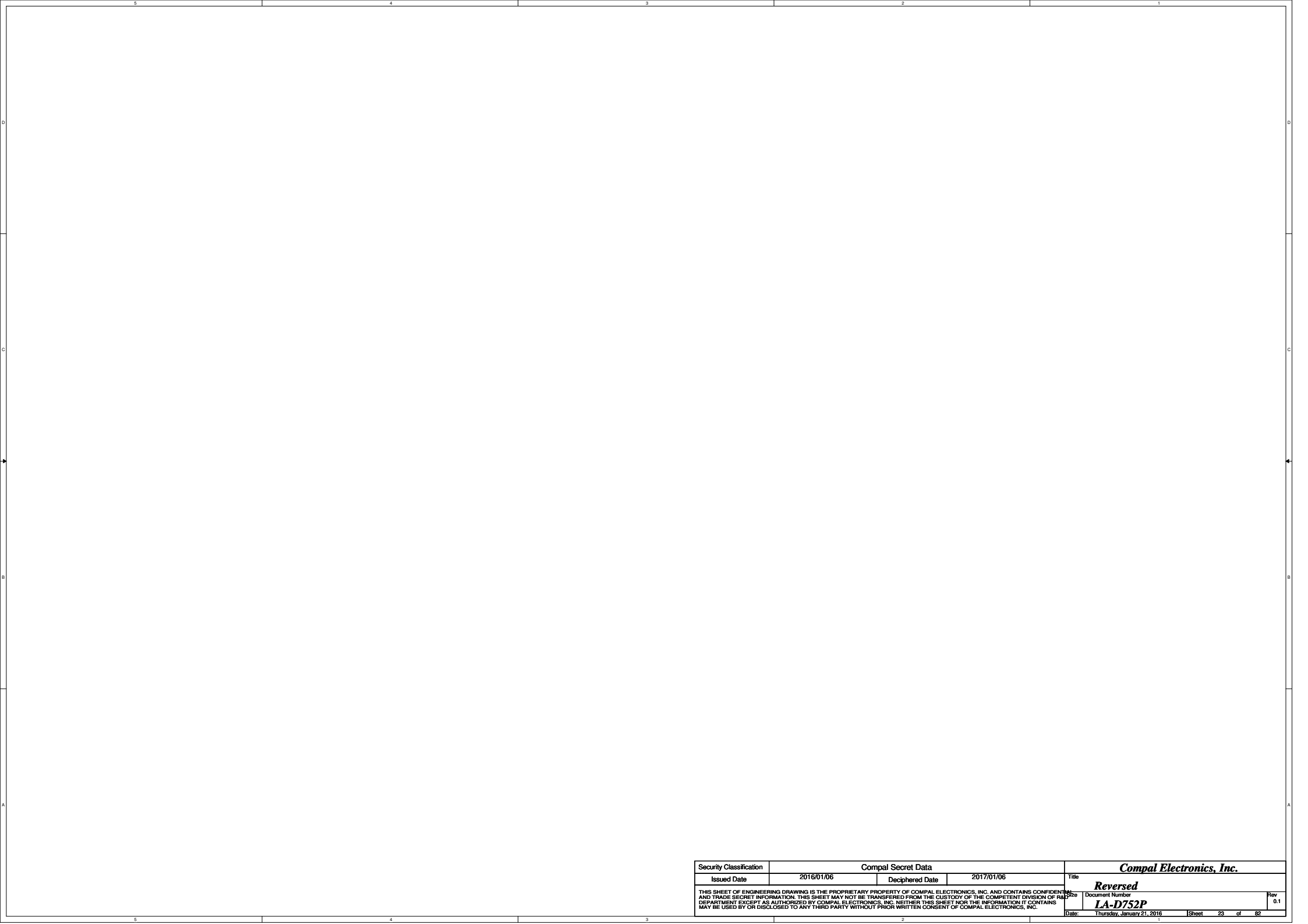
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title	PCH (4/7) DMI,PCIE,USB,LPC	
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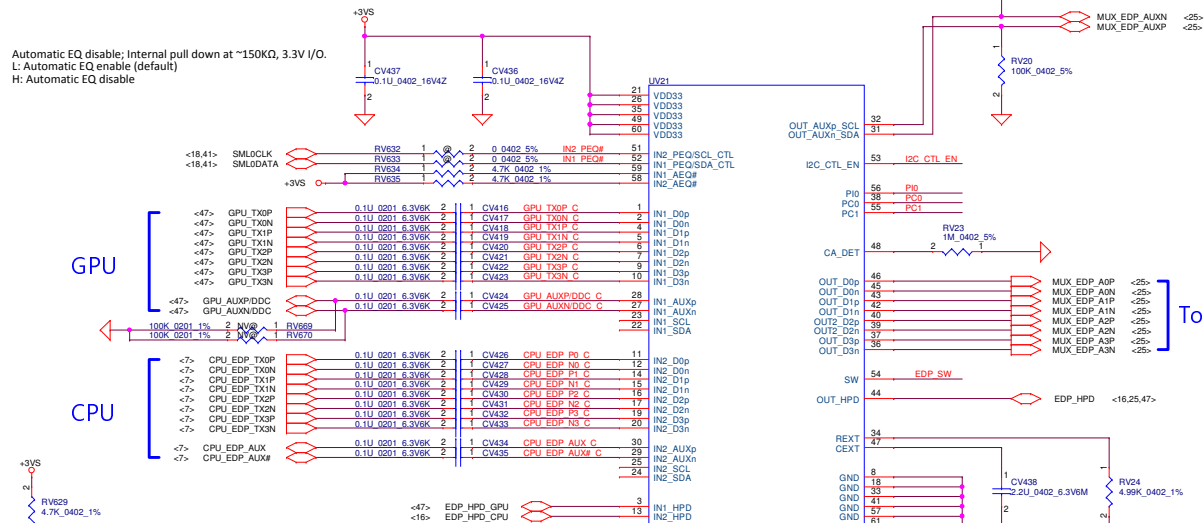


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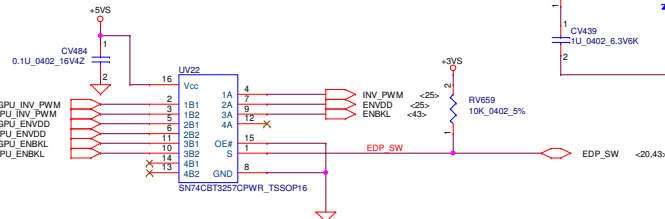
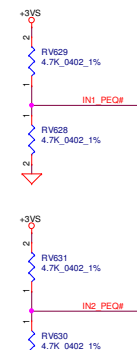




Security Classification		Compal Secret Data		Title	
Issued Date		2016/01/06	Deciphered Date	2017/01/06	
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				Document Number	0.1
				LA-D752P	
				Date: Thursday, January 21, 2016	Sheet 23 of 82

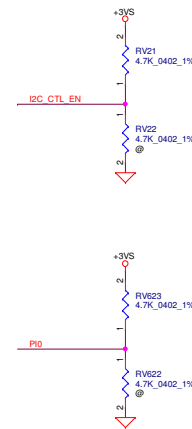


Programmable input equalization levels; Internal pull down at ~150KΩ, 3.3V I/O.  
 L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2  
 H: HEQ, compensate channel loss up to 14.5dB @ HBR2  
 M: LLEQ, compensate channel loss up to 8.5dB @ HBR2



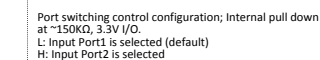
S1	OE	output	function
L	L	A=B1	IGPU
H	L	A=B2	DGPU
X	H		

To eDP connector



I2C Control Enable; Internal pull down at ~150K $\Omega$ , 3.3V I/O.  
H: I2C control is selected with default address 0x66/67  
M: I2C control is selected with alternative address 0xD8/D9

Auto test enable; Internal pull down at ~150KΩ, 3.3V I/O.  
L: Auto test disable & input offset cancellation enable (default)  
H: Auto test enable & input offset cancellation enable  
M: Auto test disable & input offset cancellation disable



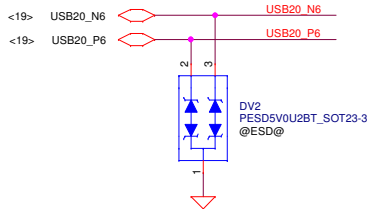
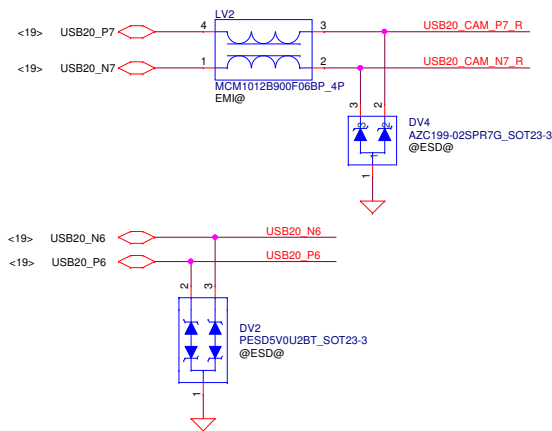
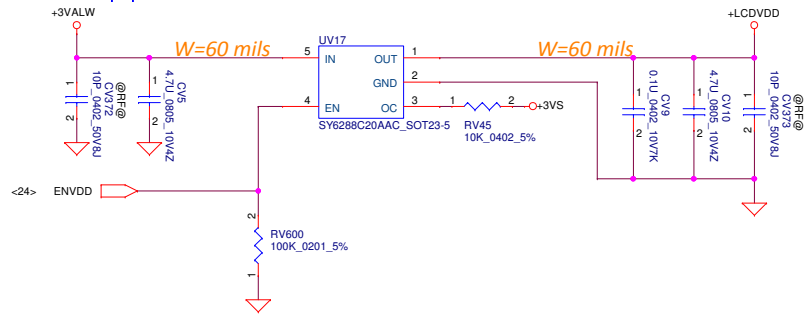
AUX interception disable for Port y (y = 1, 2). Internal pull down at ~150KΩ, 3.3V I/O;  
L: AUX interception enable, driver configuration is set by link training (default)  
H: AUX interception disable, driver output with fixed 800mV and 0dB  
M: AUX interception disable, driver output with fixed 400mV and 0dB

Output swing adjustment for Port y (y = 1, 2). Internal pull down at ~150K $\Omega$ , 3.3V I/O;  
L: default  
H: +20%  
M: -16.7%

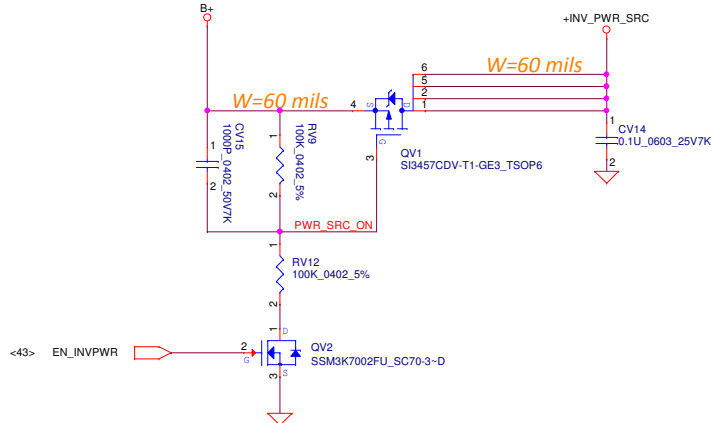


For 17" Sharp panel

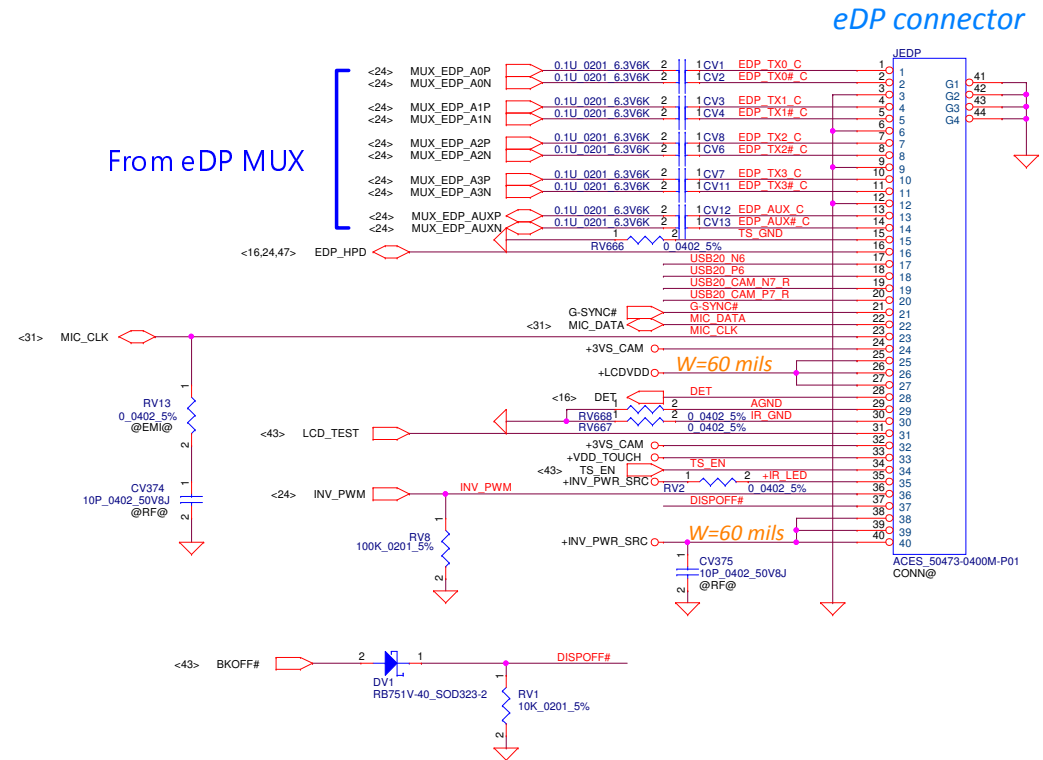
## LCD power control



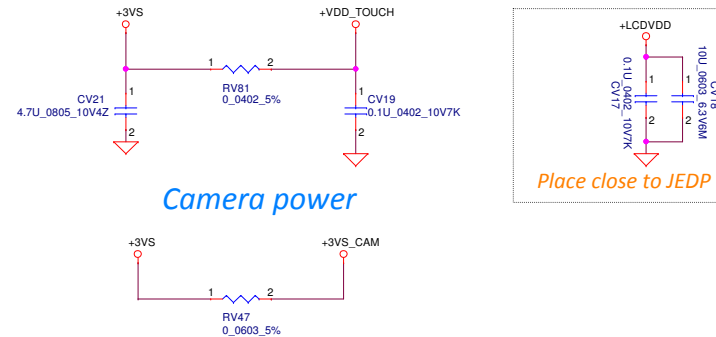
## LCD backlight power control



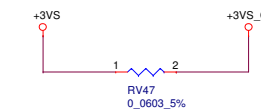
## From eDP MUX



## Touch screen panel power

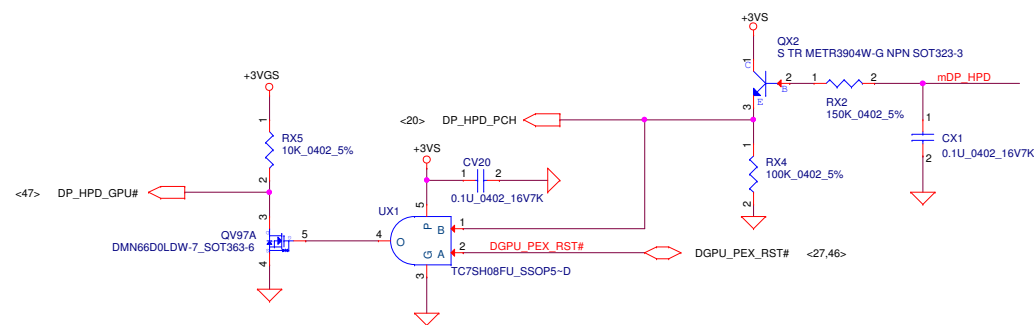
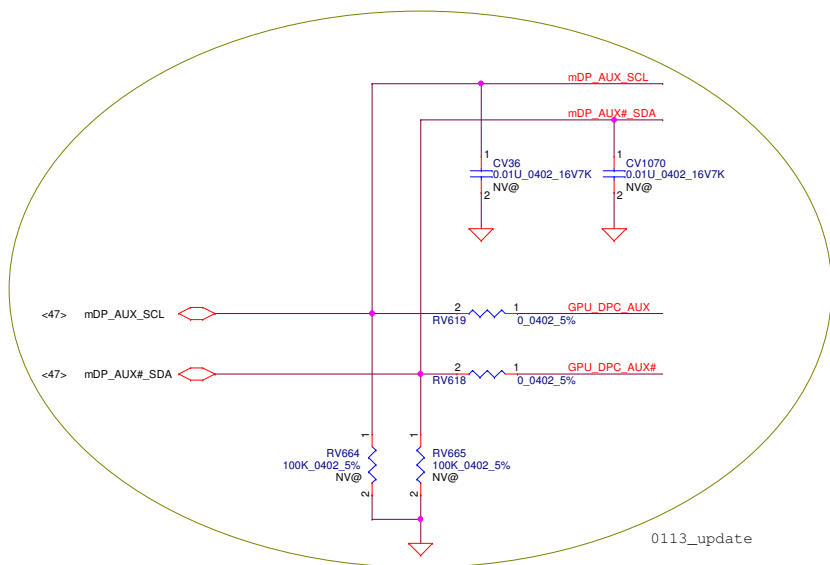
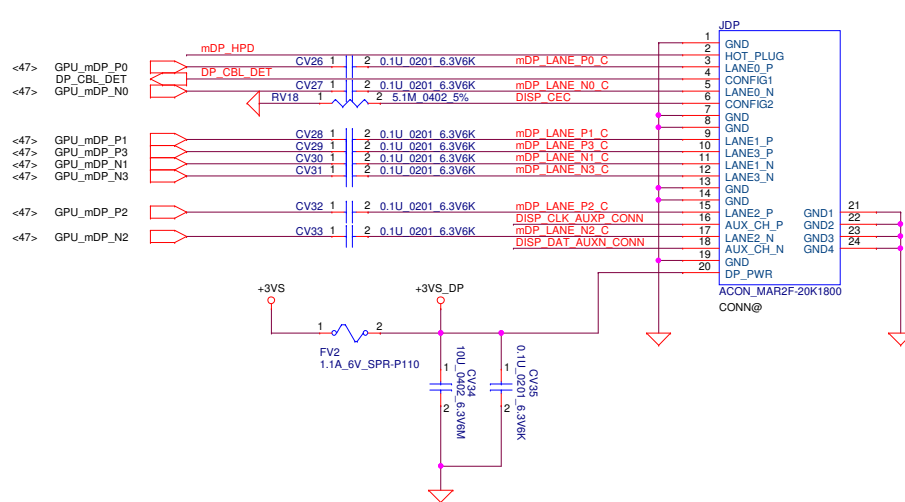
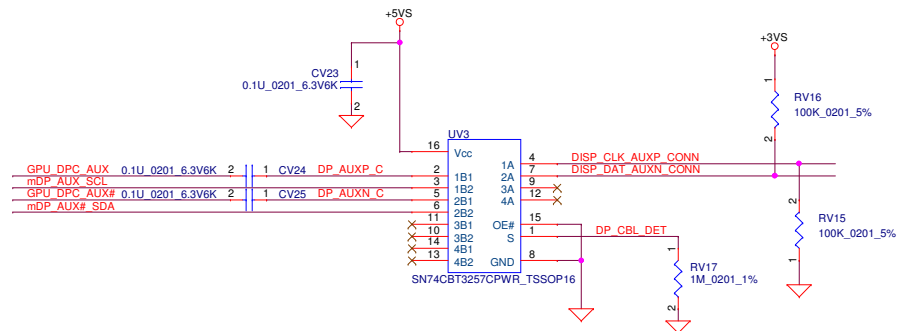


## Camera power

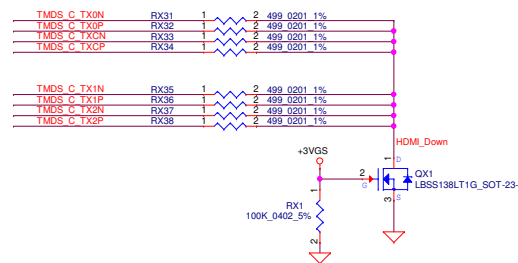
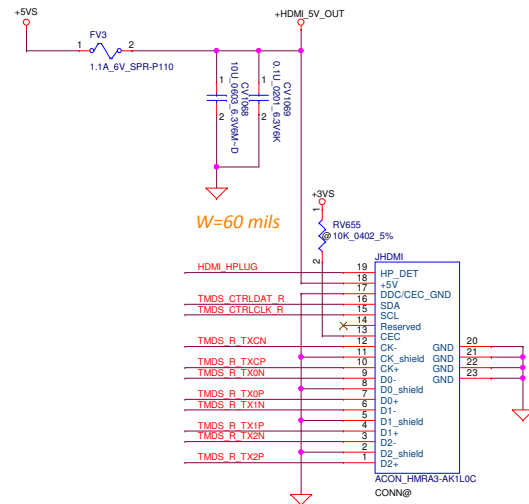
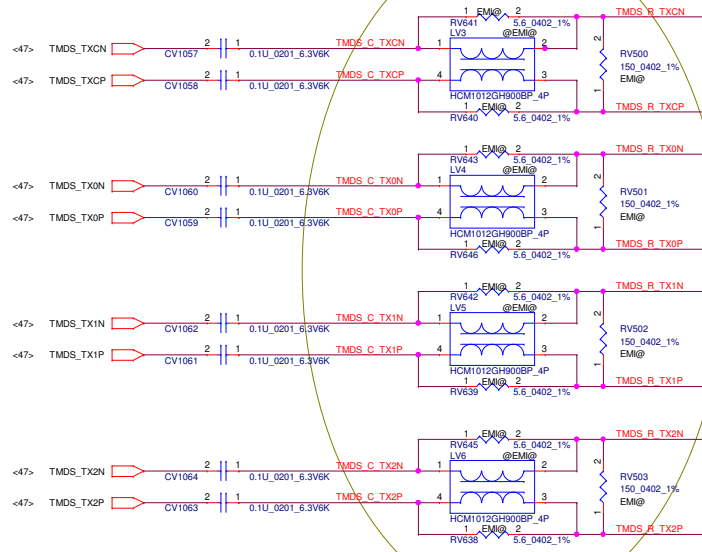


IR camera pindefine :  
 IR\_LED+  
 IR\_LED-  
 IR\_LED+/NC  
 IR\_LED-/DET , connect to PCH GPIO  
 IR\_LED-  
 Diglog\_loop , connect to PCH GPIO  
 DGND  
 D+  
 D-  
 USB3V3  
 MIC\_SIG  
 MIC\_CLK  
 DGND

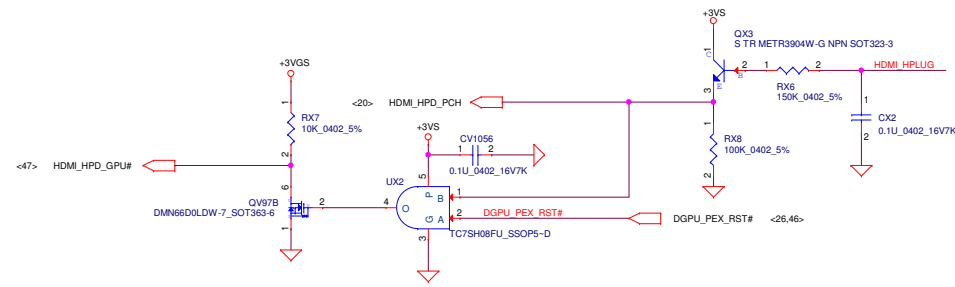
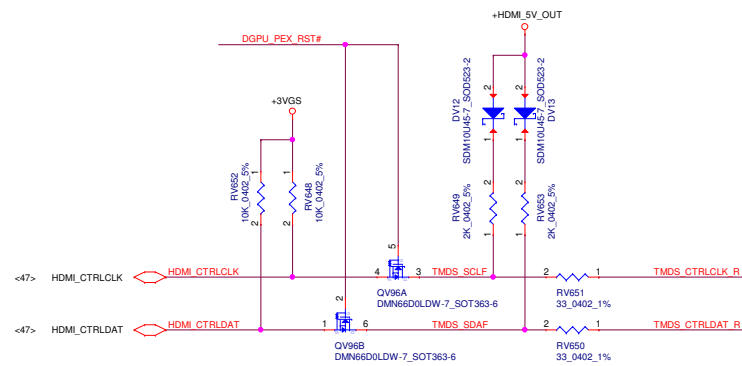
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Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title	eDP/Camera/TS	
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				LA-D752P		
				Date:	Thursday, January 21, 2016	Sheet 25 of 82



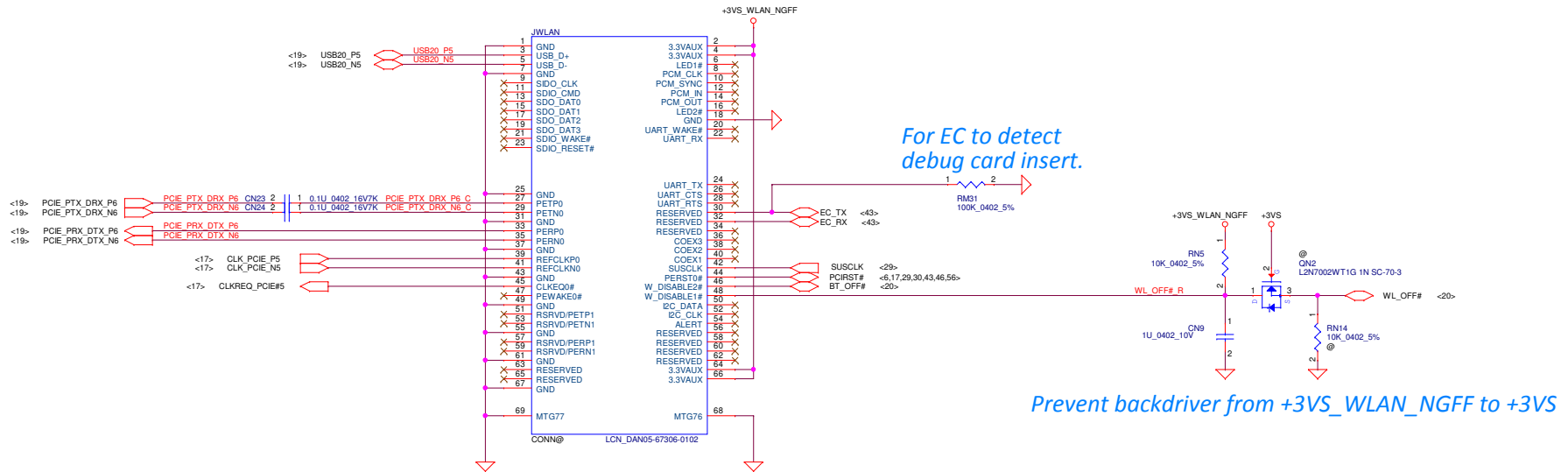
Reserve LV3,LV4,LV5,LV6 co-lay with EMI solution @ 01/12



To GPU



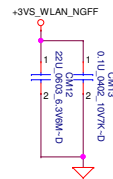
# M.2 2230 slot(type E)



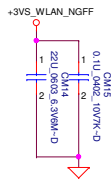
For EC to detect debug card insert.

Prevent backdriver from +3VS\_WLAN\_NGFF to +3VS

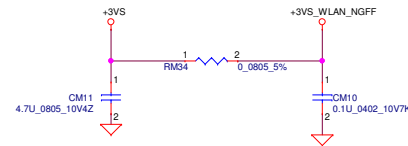
closed to pin 2, 4



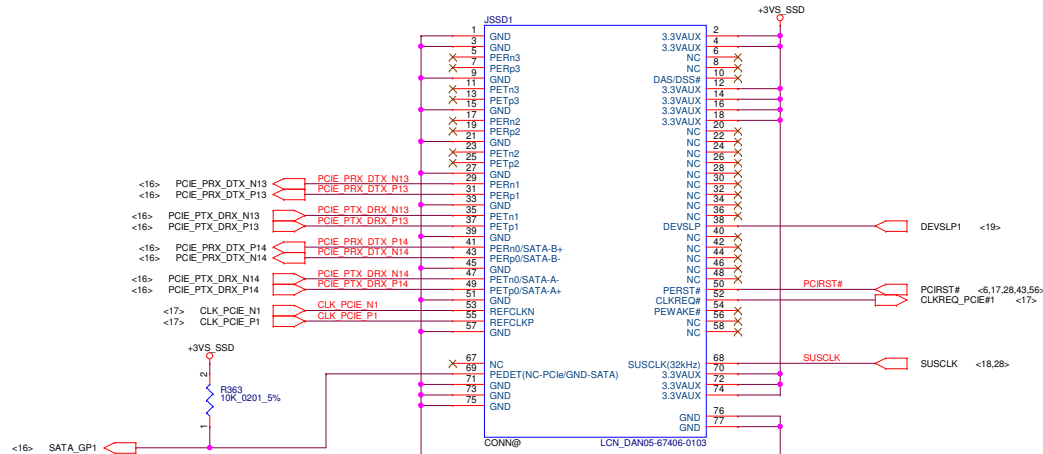
closed to pin 64, 66



WLAN power control

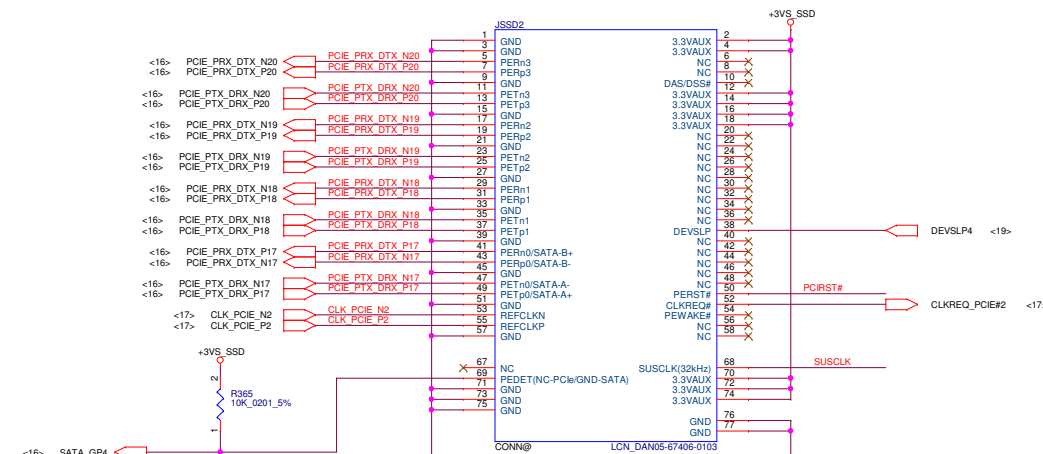


# PCIe/SATA SSD NGFF Slot\_1 Key M



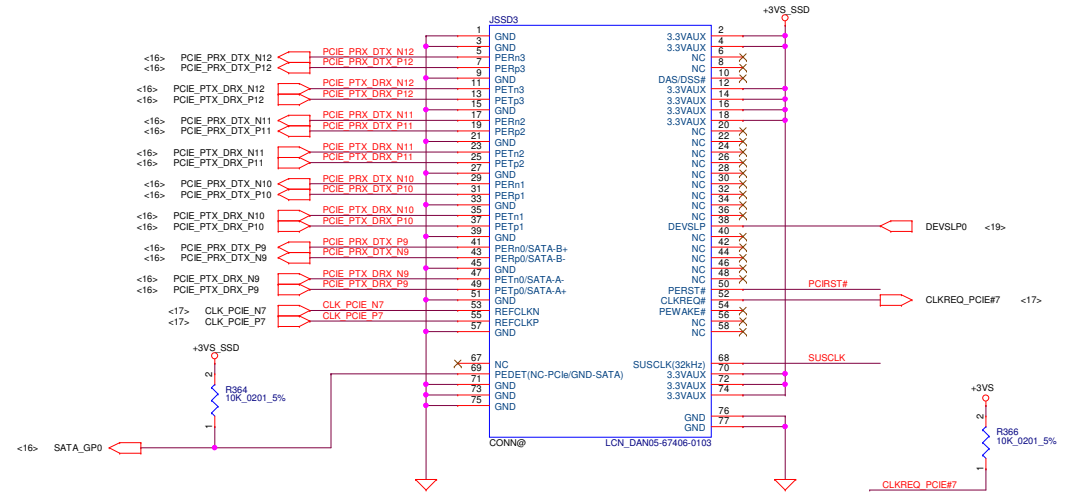
PEDET	Module Type
0	SATA
1	PCIe

# PCIe/SATA SSD NGFF Slot\_2 Key M

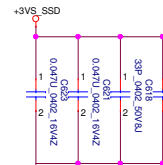


PEDET	Module Type
0	SATA
1	PCIe

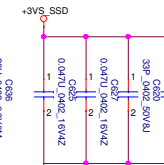
# PCIe/SATA SSD NGFF Slot\_3 Key M



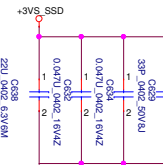
## JSSD1



## JSSD2

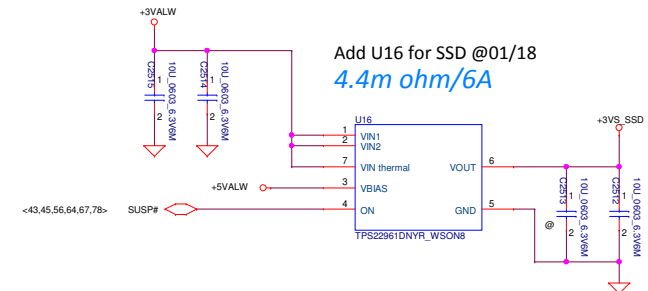


## JSSD3

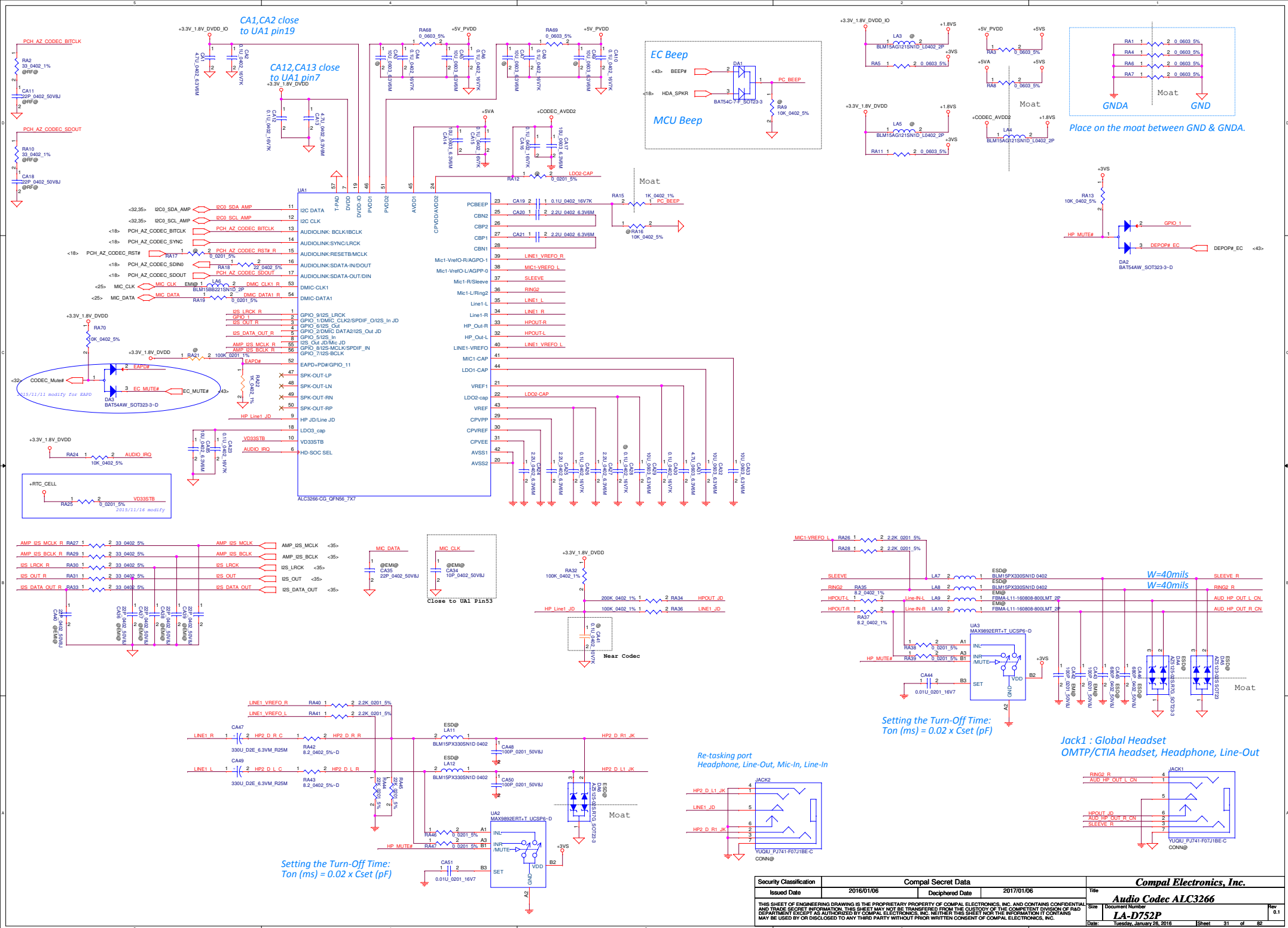


Delete C619,C626 @12/29  
C622,C624 from 0805 to 0402 @01/08  
Add 22U C635,C636,C637,C638,C639,C640 @01/08

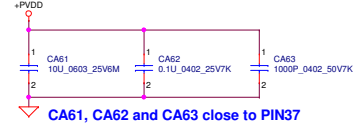
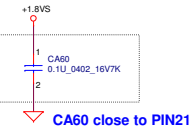
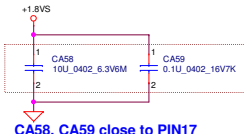
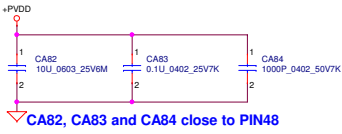
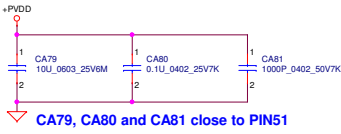
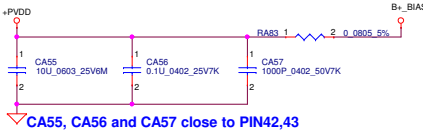
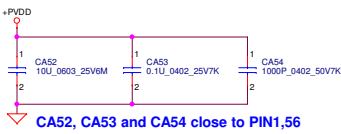
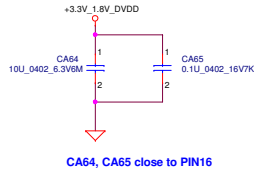
Add U16 for SSD @01/18  
4.4m ohm/6A



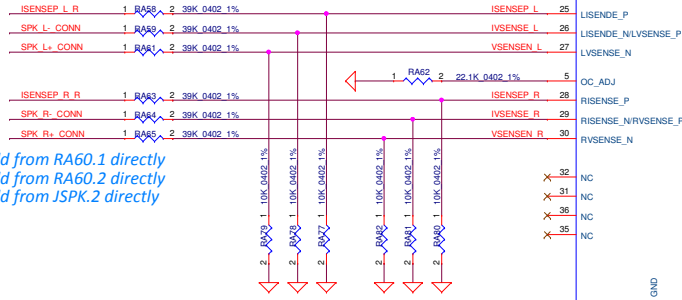




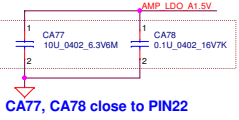
SMART AMP



RA58.1 should from RA57.1 directly  
RA59.1 should from RA57.2 directly  
RA61.1 should from JSPK.4 directly



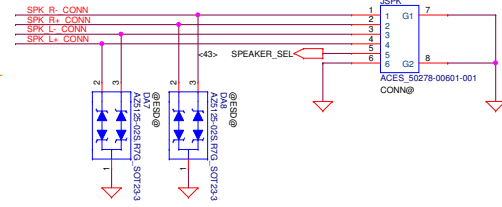
RA63.1 should from RA60.1 directly  
RA64.1 should from RA60.2 directly  
RA65.1 should from JSPK.2 directly



Int. Speaker Conn.

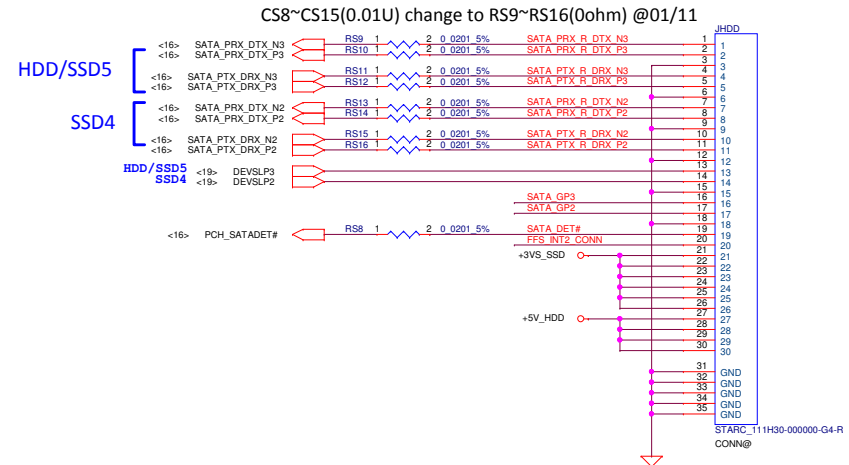
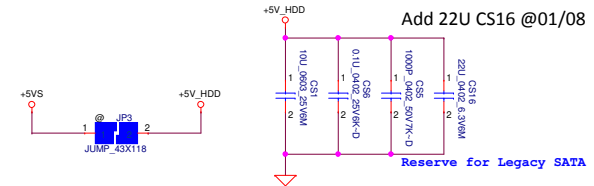
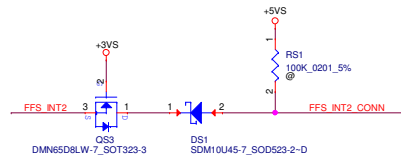
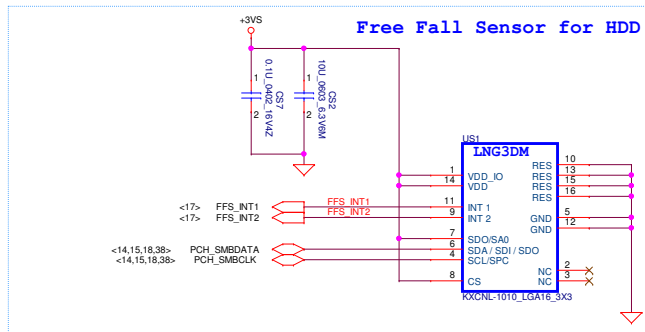
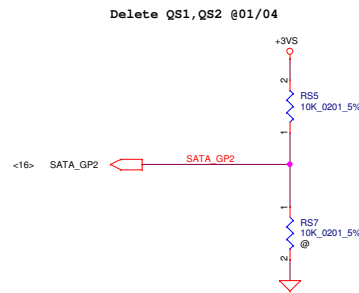
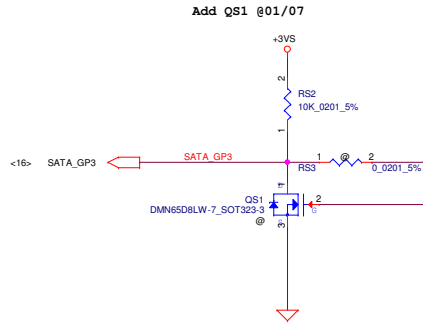
40 mils = For 4 ohm 3W Speaker  
Close to UA1 Pin42,43,44,45

Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-  
Speaker 4 ohm : 40 mil  
Speaker 8 ohm : 20 mil

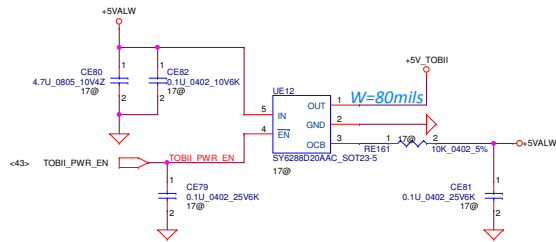


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Date: Tuesday, January 26, 2016					Sheet 32 of 82

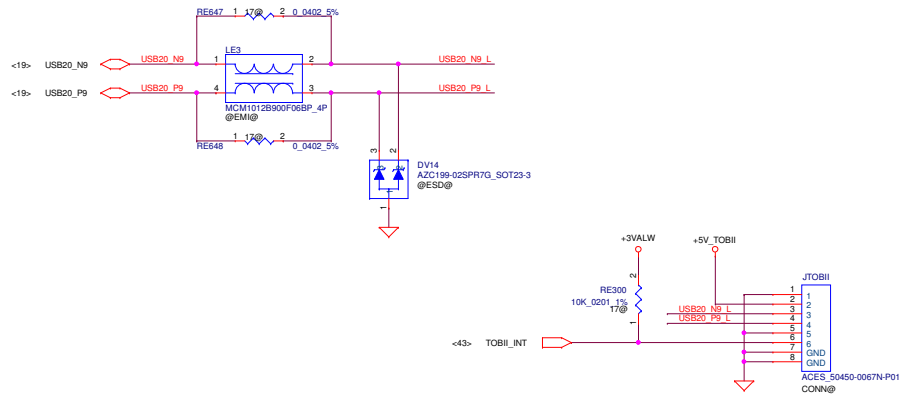




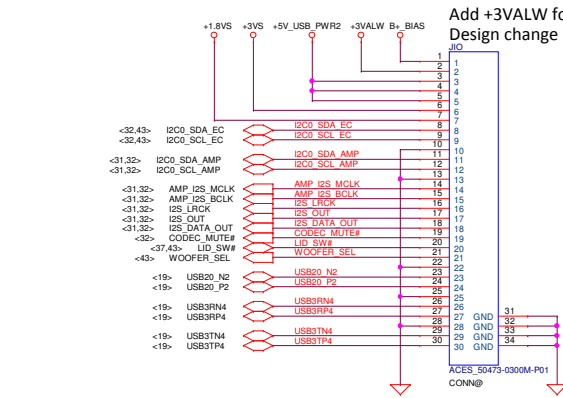
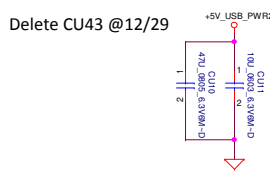
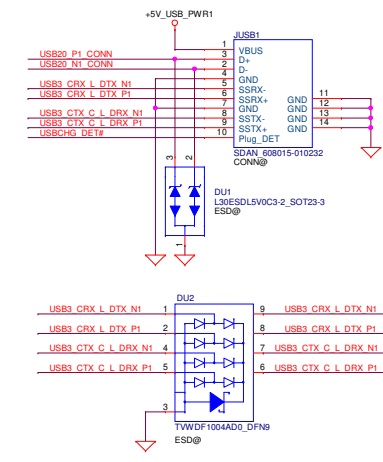
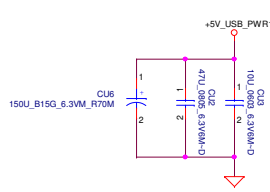
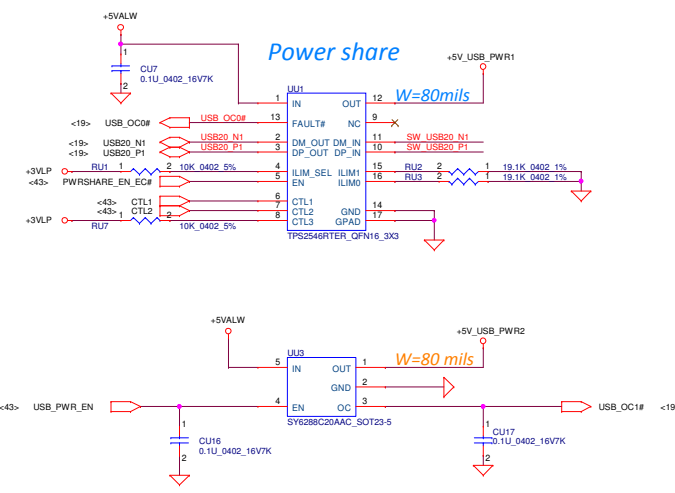
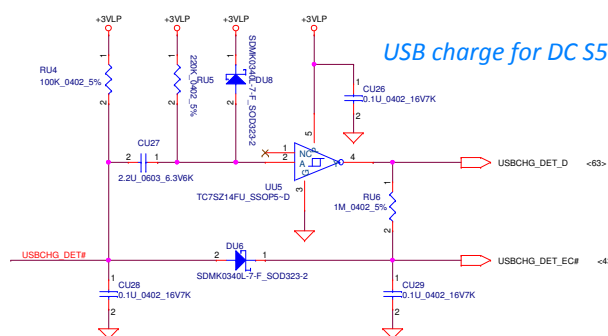
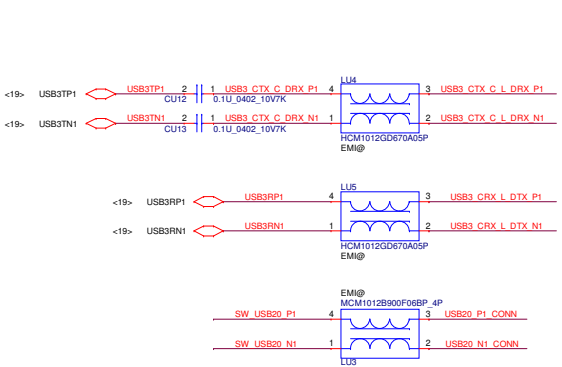
**Tobii Conn.**

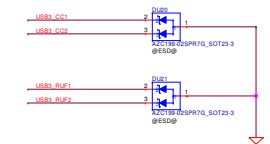
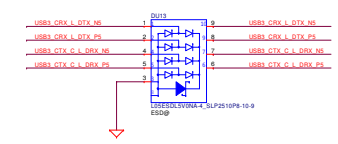
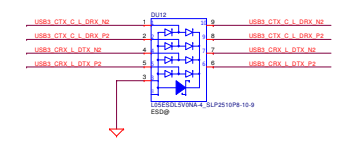
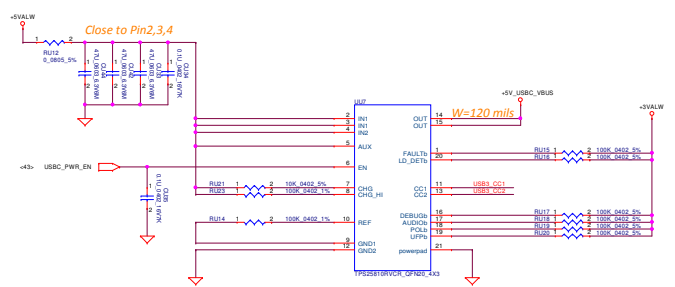
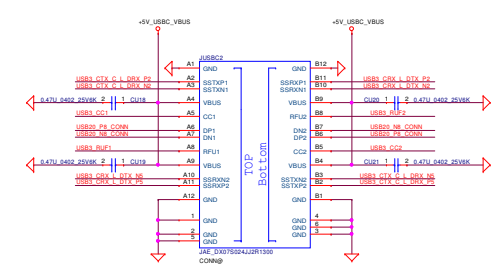
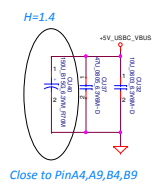
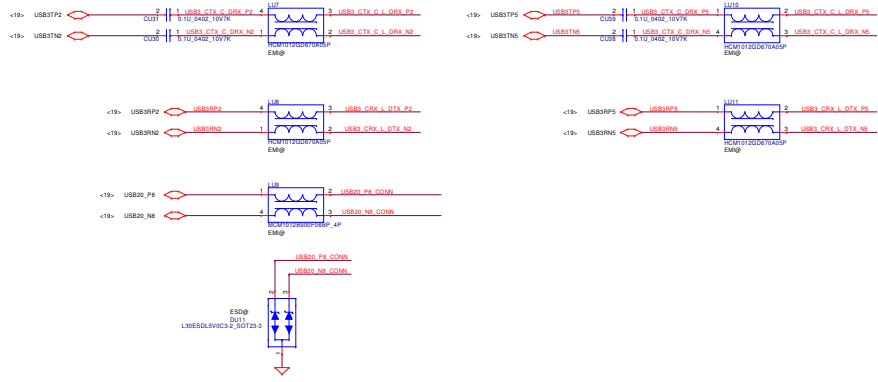


*Near JTOBII*

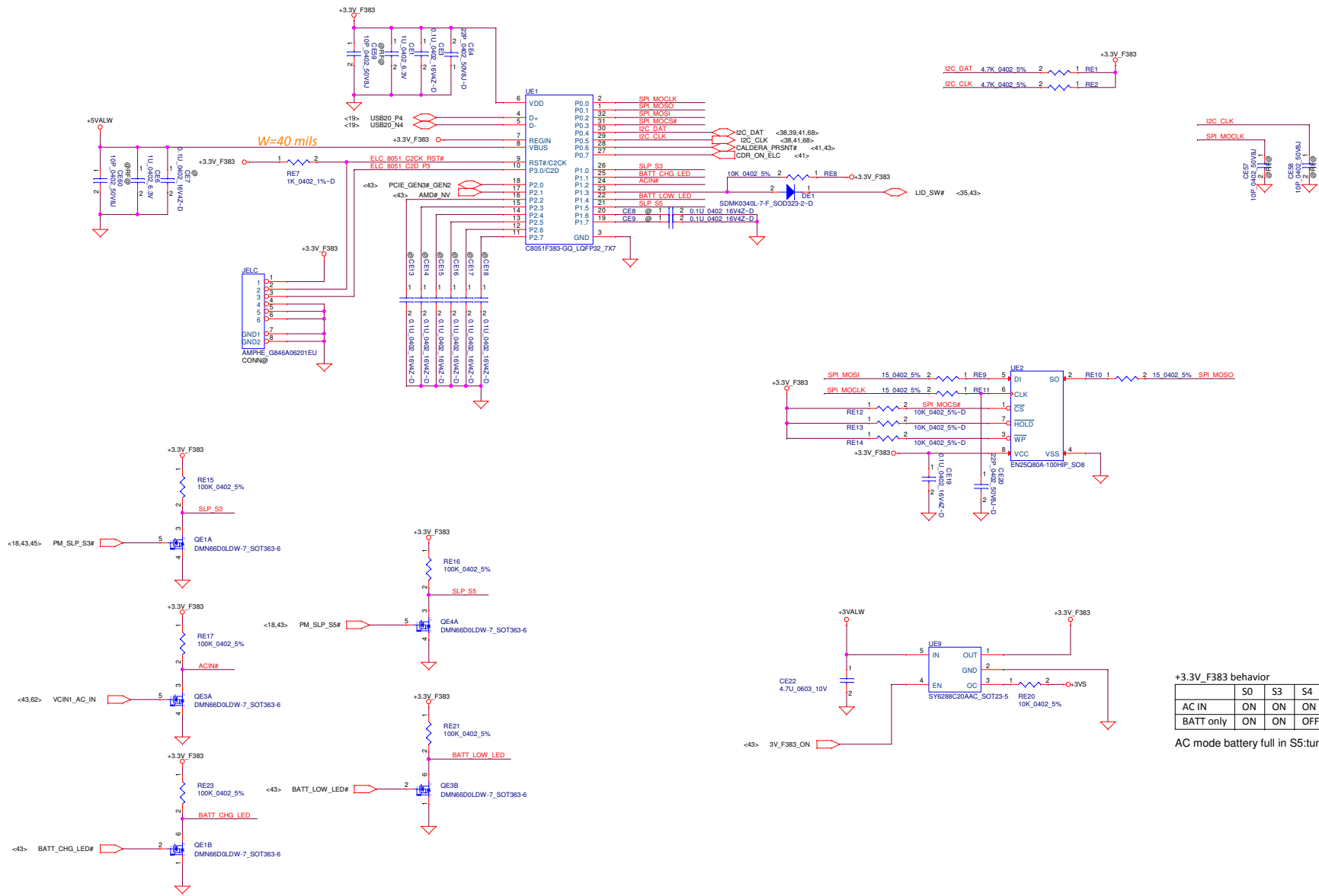


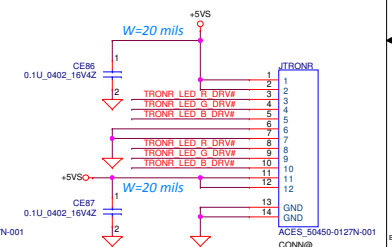
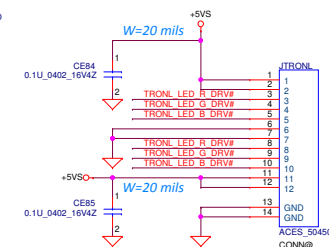
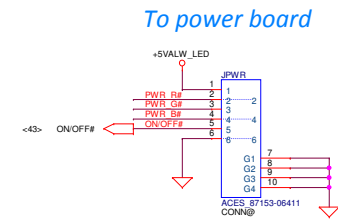
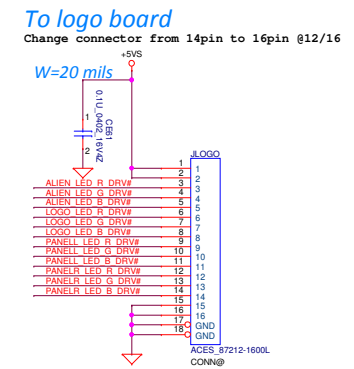
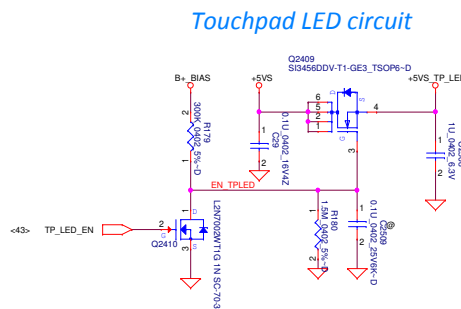
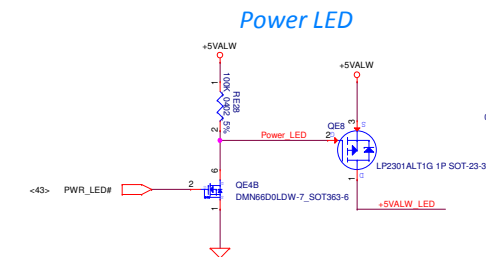
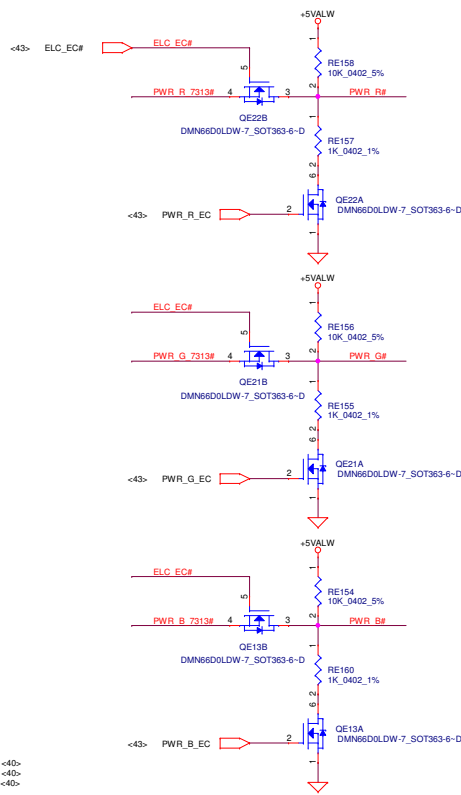
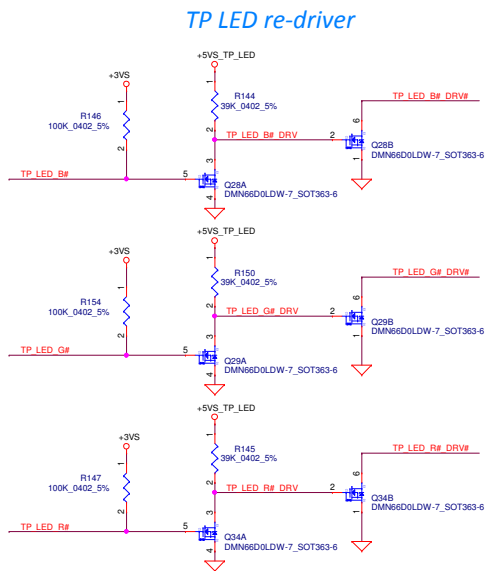
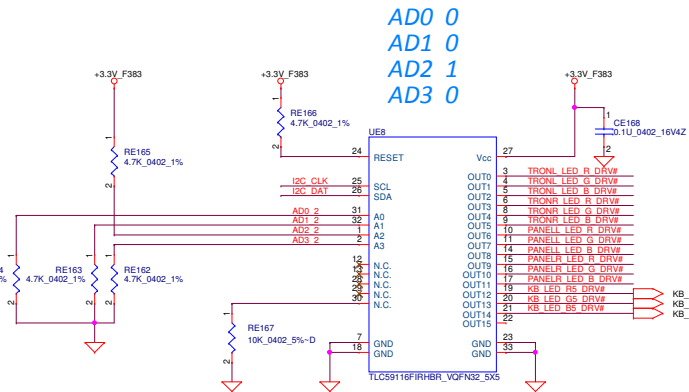
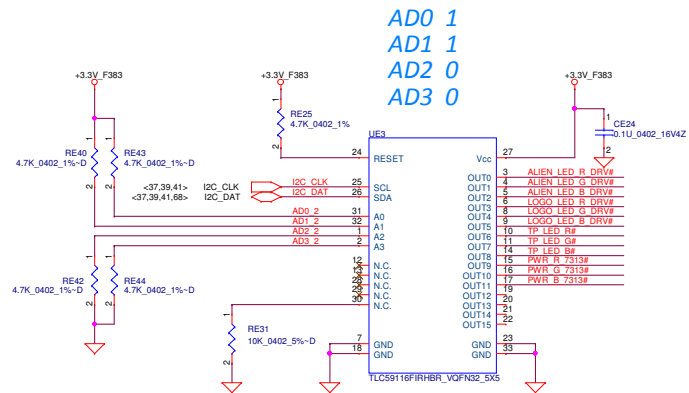
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Issued Date	2016/01/06	Deciphered Date	2017/01/06	<b>Tobii (T7) Only</b> Documented by: <b>LA-D752P</b>	
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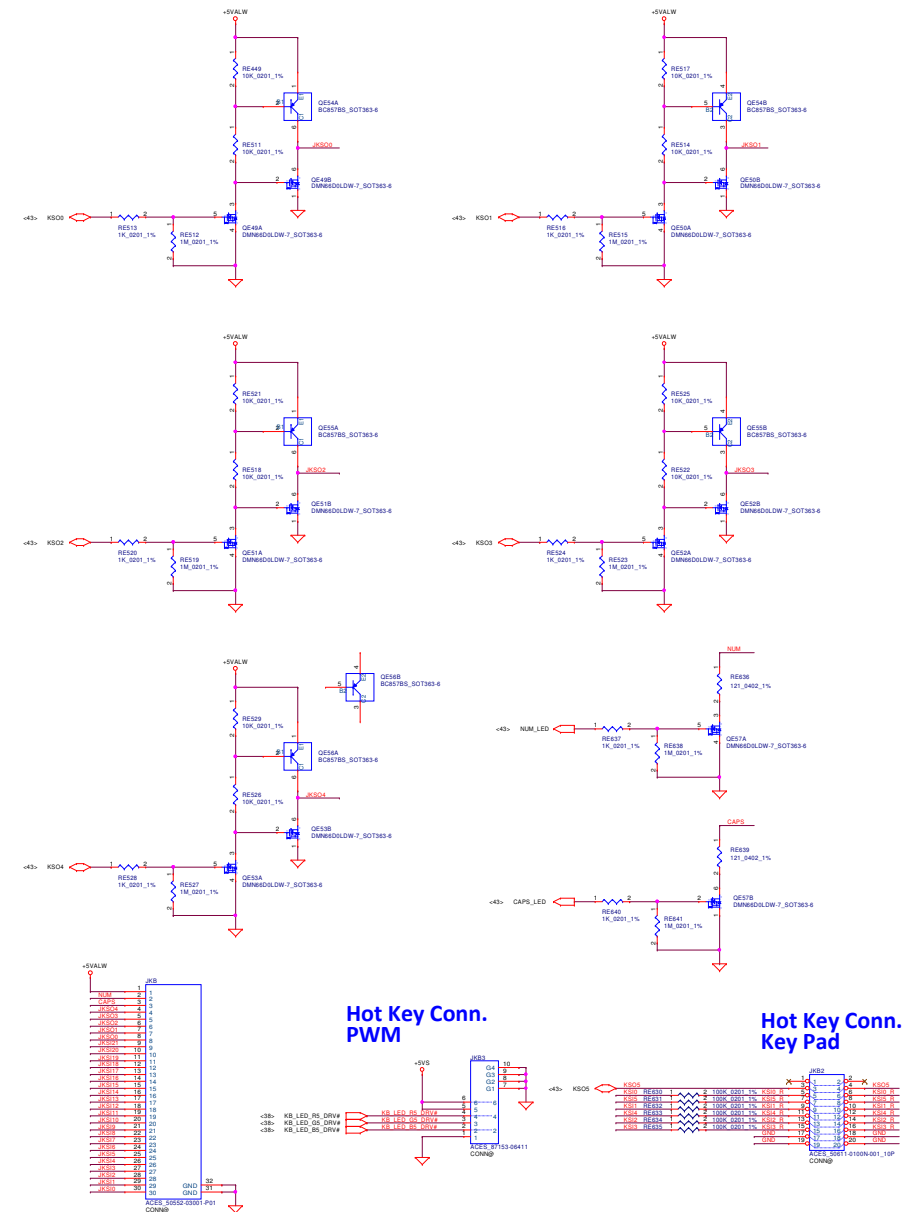
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2016/01/06	Discontinued Date	2017/01/06	Type	USB3.0/2.0 (TypeC)
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LA-D752P				Date	Thursday, January 21, 2016
				Drawn	08 of 02





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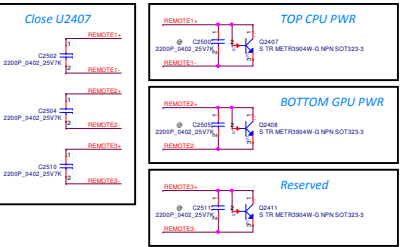
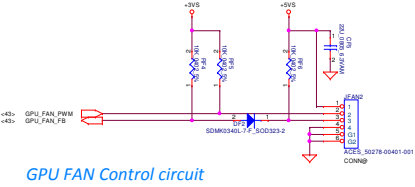




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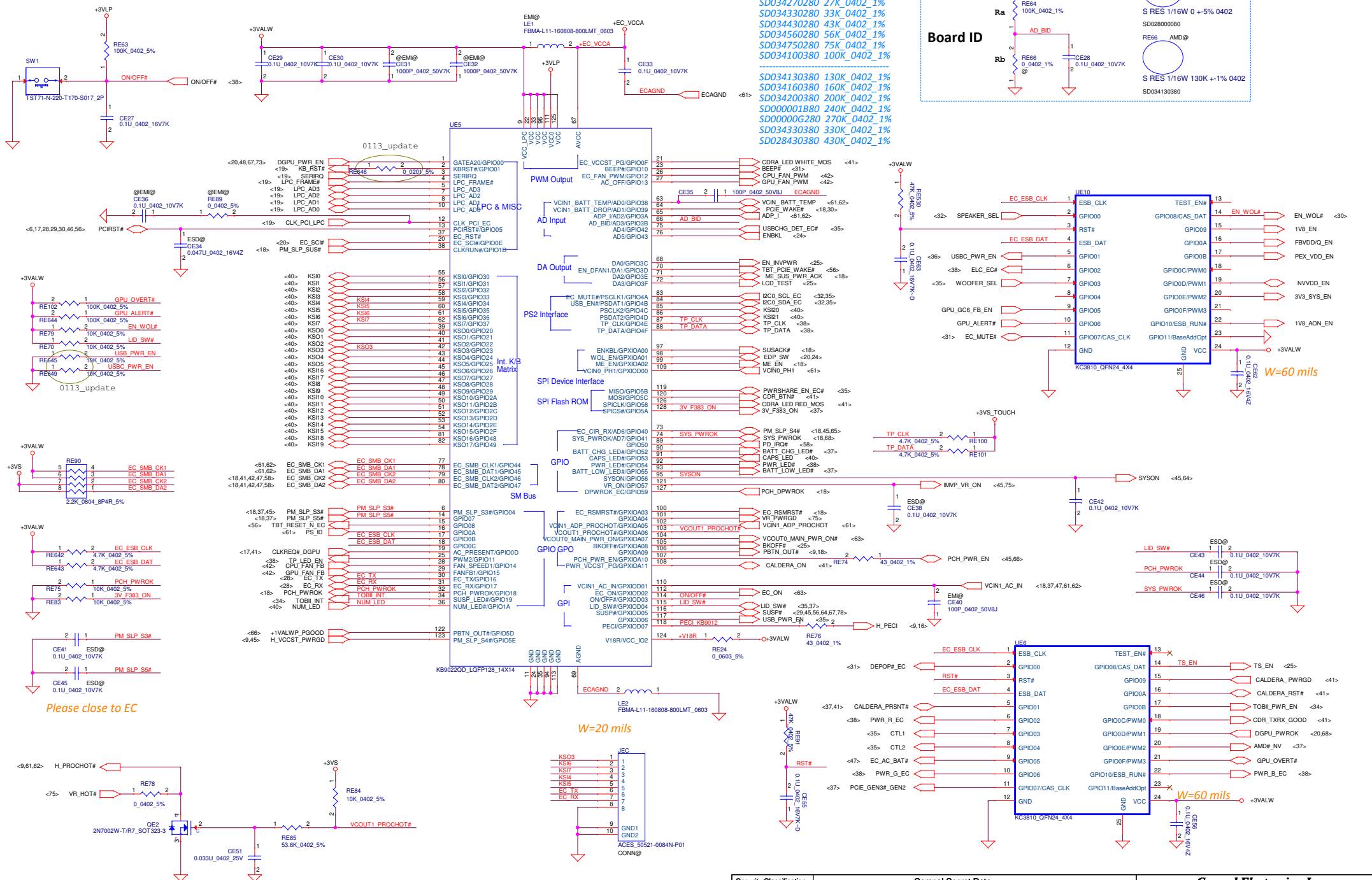




[illegible]

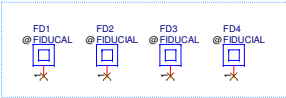
Security Classification		Control Secret Data		Comptel Electronics, Inc.	
Issued Date		Declassified Date		Title	
2016/6/06		2017/0/06		FAN/Thermal	
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1		LA-D752P		0.1	
Date		Issued		Page	
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### Power ON circuit

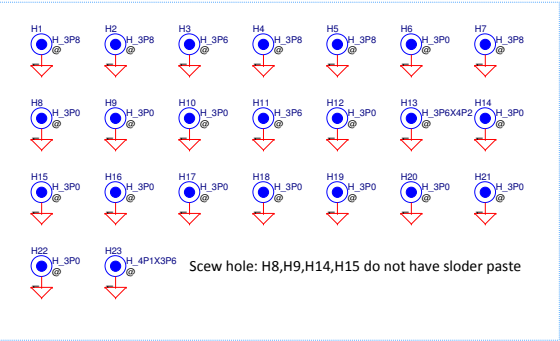


Security Classification		Compal Secret Data		<i><b>Compal Electronics, Inc.</b></i>	
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title	<i><b>EC ENE-KB9022</b></i>
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				Document Number <i><b>LA-D752P</b></i>	
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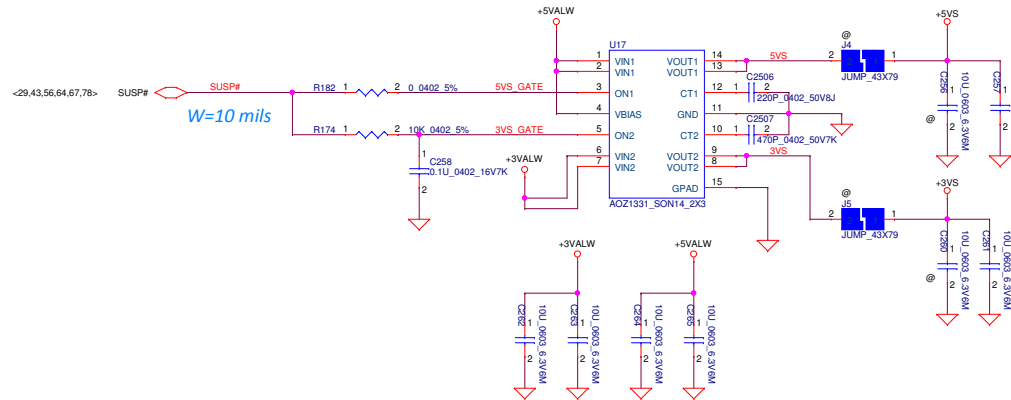
Fiducial Mark



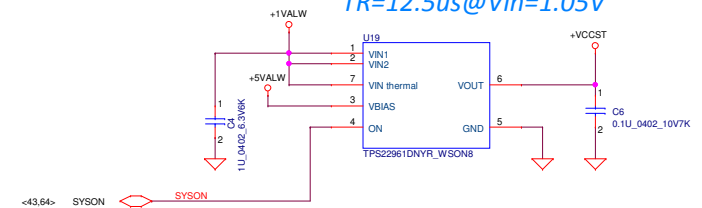
PCB Screw Hole



+5VS and +3VS switch  
20mohm/6A per channel

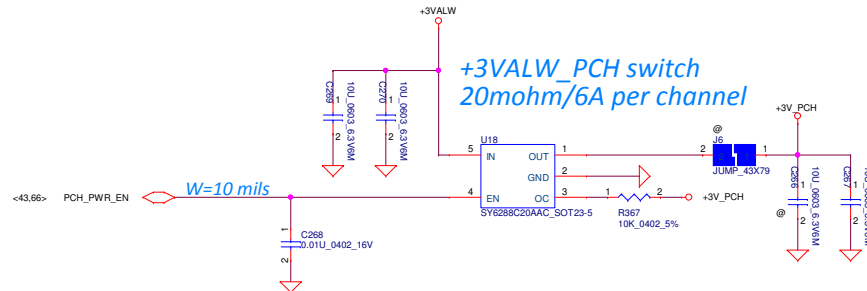


+VCCST switch  
4.4mohm/6A  
TR=12.5us@Vin=1.05V

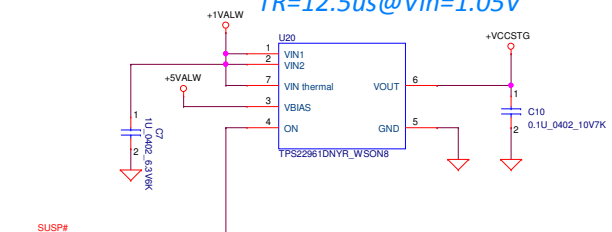


Main source TI SA00007XR00 (\$ IC TPS22961DNYR WSON 8P LOAD SWITCH)  
2nd source AOS SA00008A800 (\$ IC AOZ1334DI-01 DFN 8P SINGLE LOAD SW)  
3rd source EMC SA00008R600 (\$ IC EM5201V DFN3X3 8P LOAD SWITCH)  
4st source APEC SA00006V300 (\$ IC APE8939GN3 DFN 8P LOAD SWITCH)

+3VALW\_PCH switch  
20mohm/6A per channel



+VCCSTG switch  
4.4mohm/6A  
TR=12.5us@Vin=1.05V

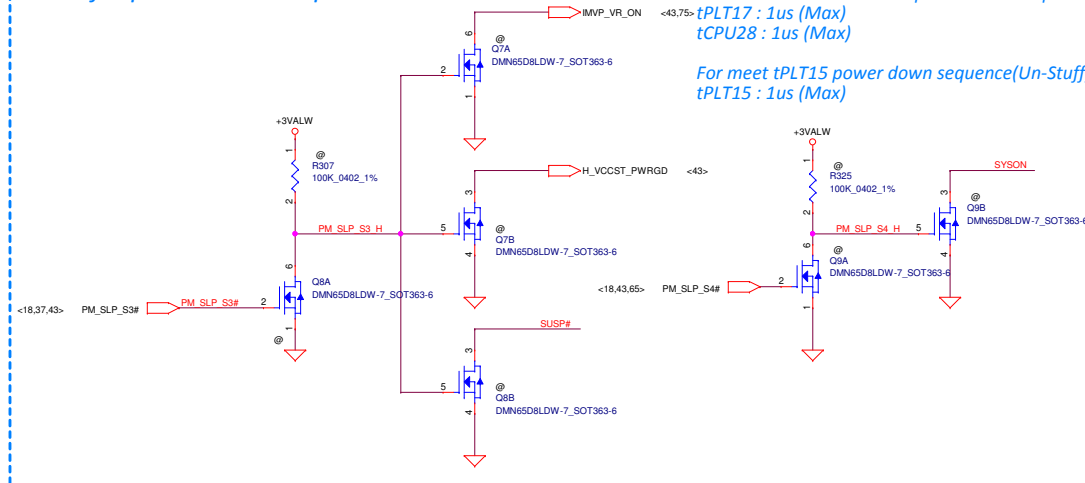


Main source TI SA00007XR00 (\$ IC TPS22961DNYR WSON 8P LOAD SWITCH)  
2nd source AOS SA00008A800 (\$ IC AOZ1334DI-01 DFN 8P SINGLE LOAD SW)  
3rd source EMC SA00008R600 (\$ IC EM5201V DFN3X3 8P LOAD SWITCH)  
4st source APEC SA00006V300 (\$ IC APE8939GN3 DFN 8P LOAD SWITCH)

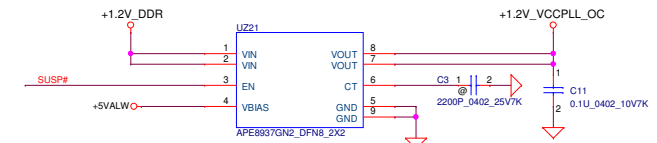
add for power down sequence

For meet tPLT17 & tCPU28 power down sequence.  
tPLT17 : 1us (Max)  
tCPU28 : 1us (Max)

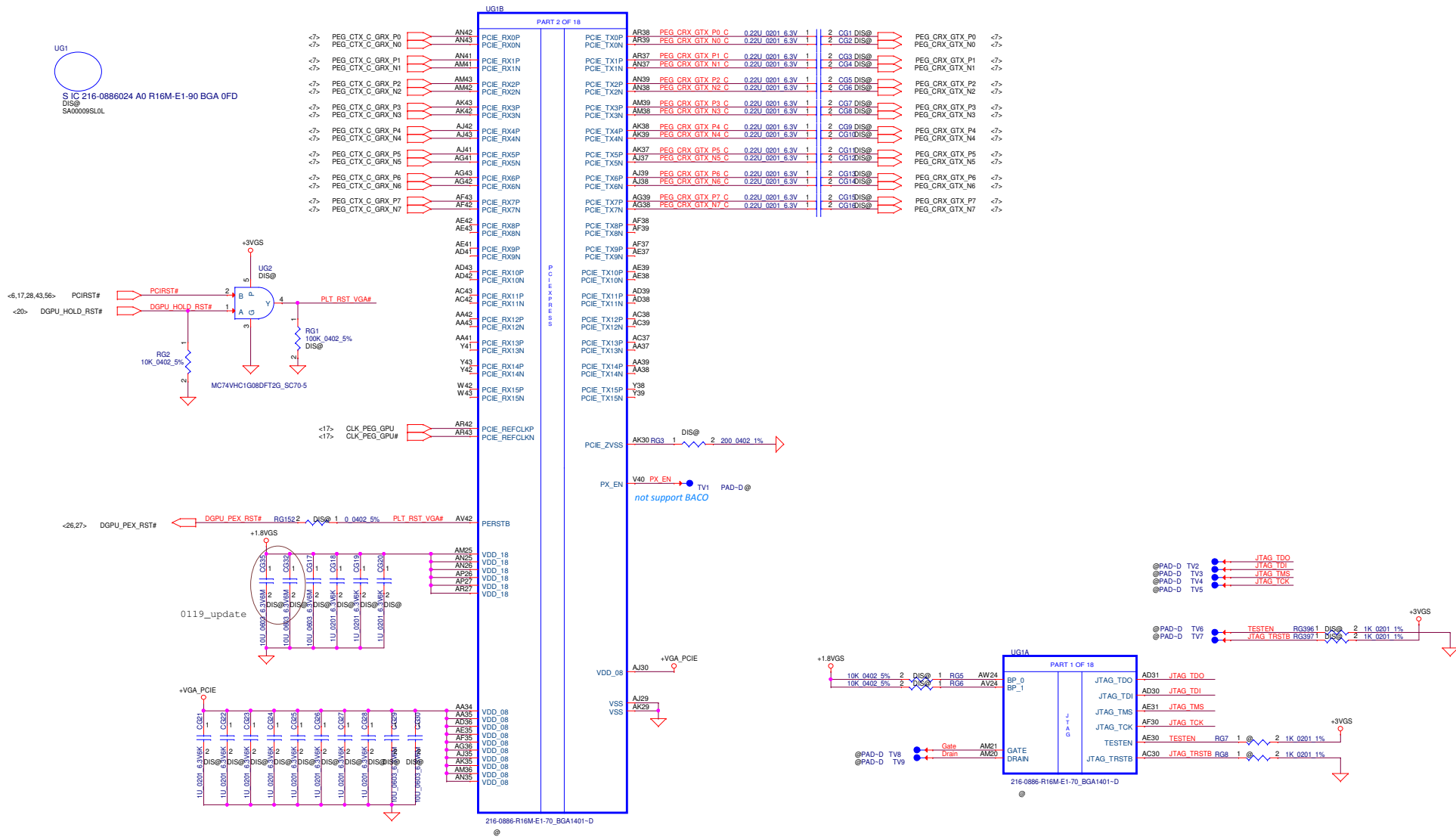
For meet tPLT15 power down sequence(Un-Stuff)  
tPLT15 : 1us (Max)

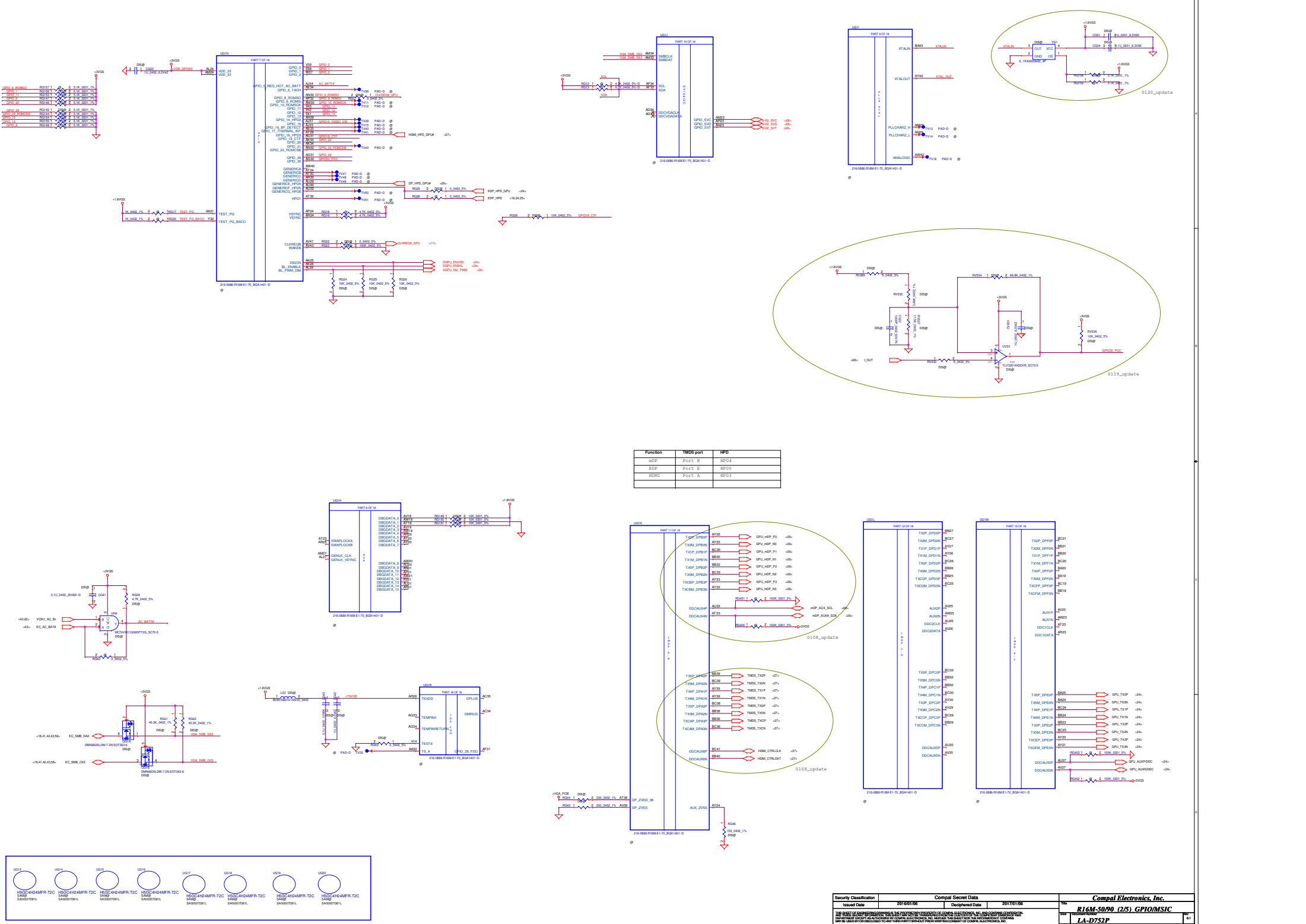


+1.2V\_VCCPLL\_OC switch  
22mohm/4A  
TR=520us@Vin=0.8V



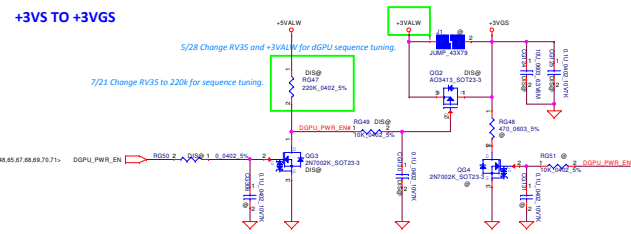
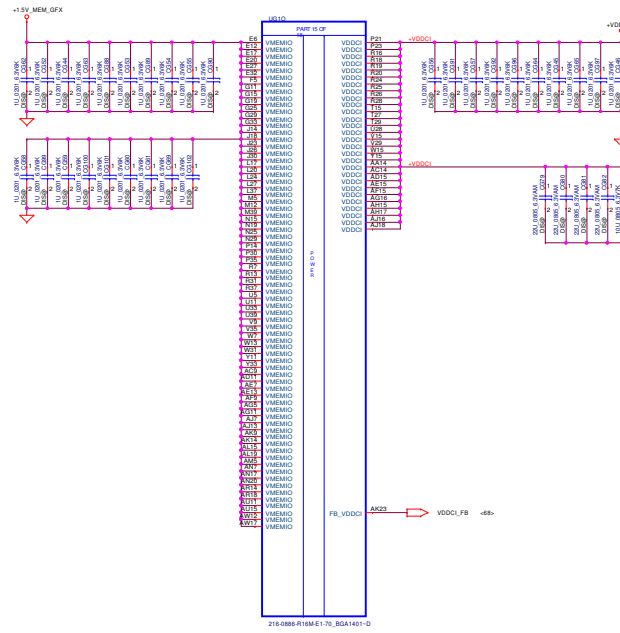
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				Date: Thursday, January 21, 2016	Sheet 45 of 82



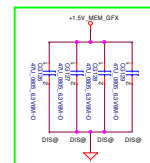


Function	TMOS pin	WFO
MDP	Port: B	BP04
BDP	Port: E	BP05
BDH1	Port: A	BP03

<43,48,65,67,68,69,70,71> DGPU\_PWR\_EN  DRVN <68>

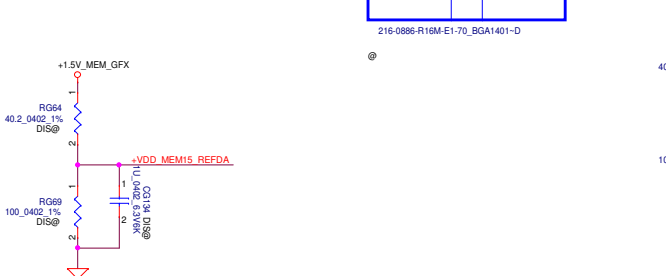
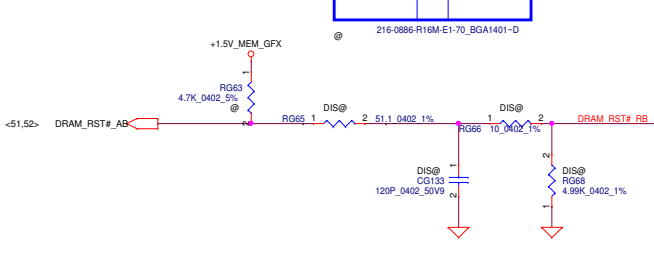


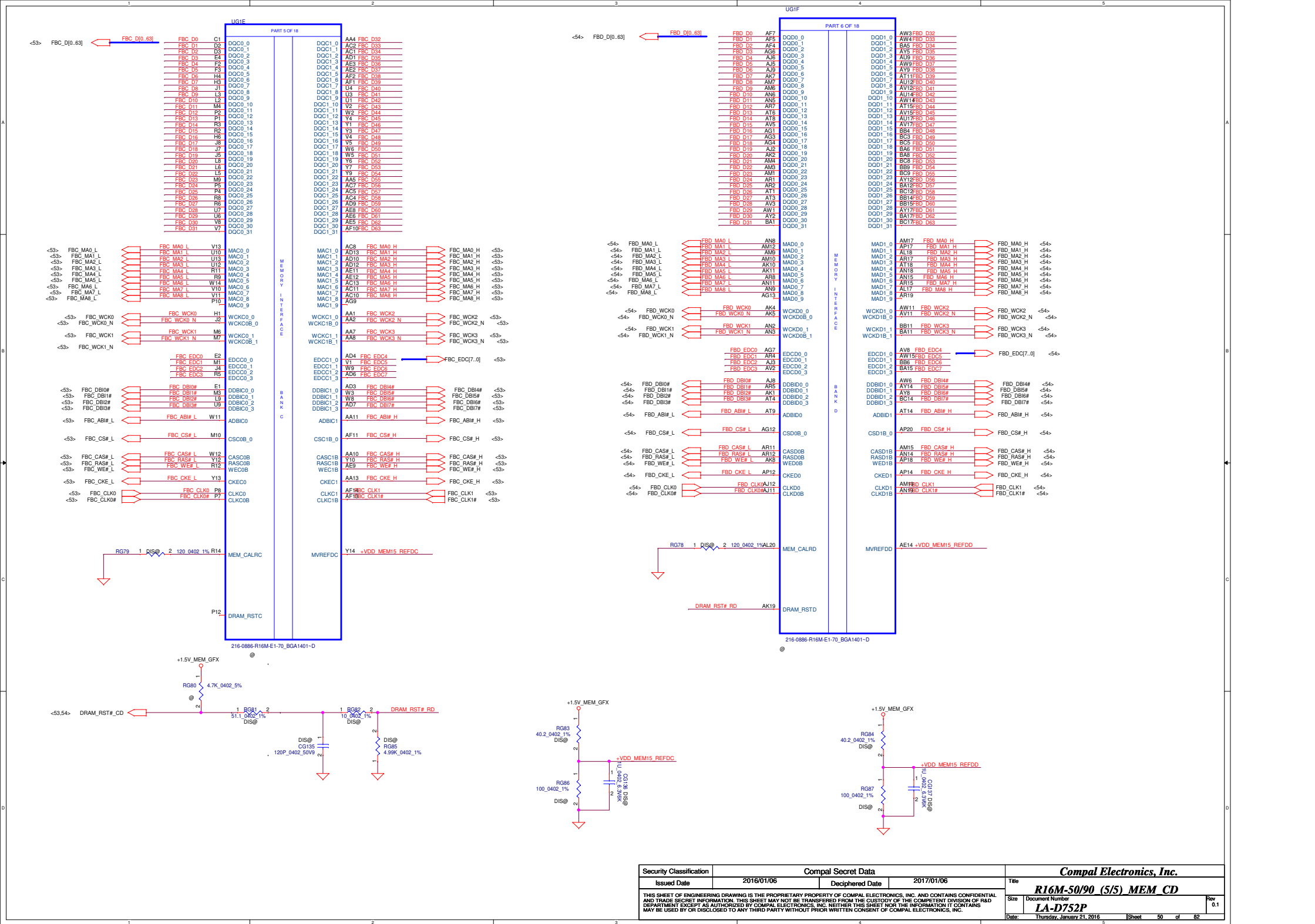
## SHORT DEFAULT



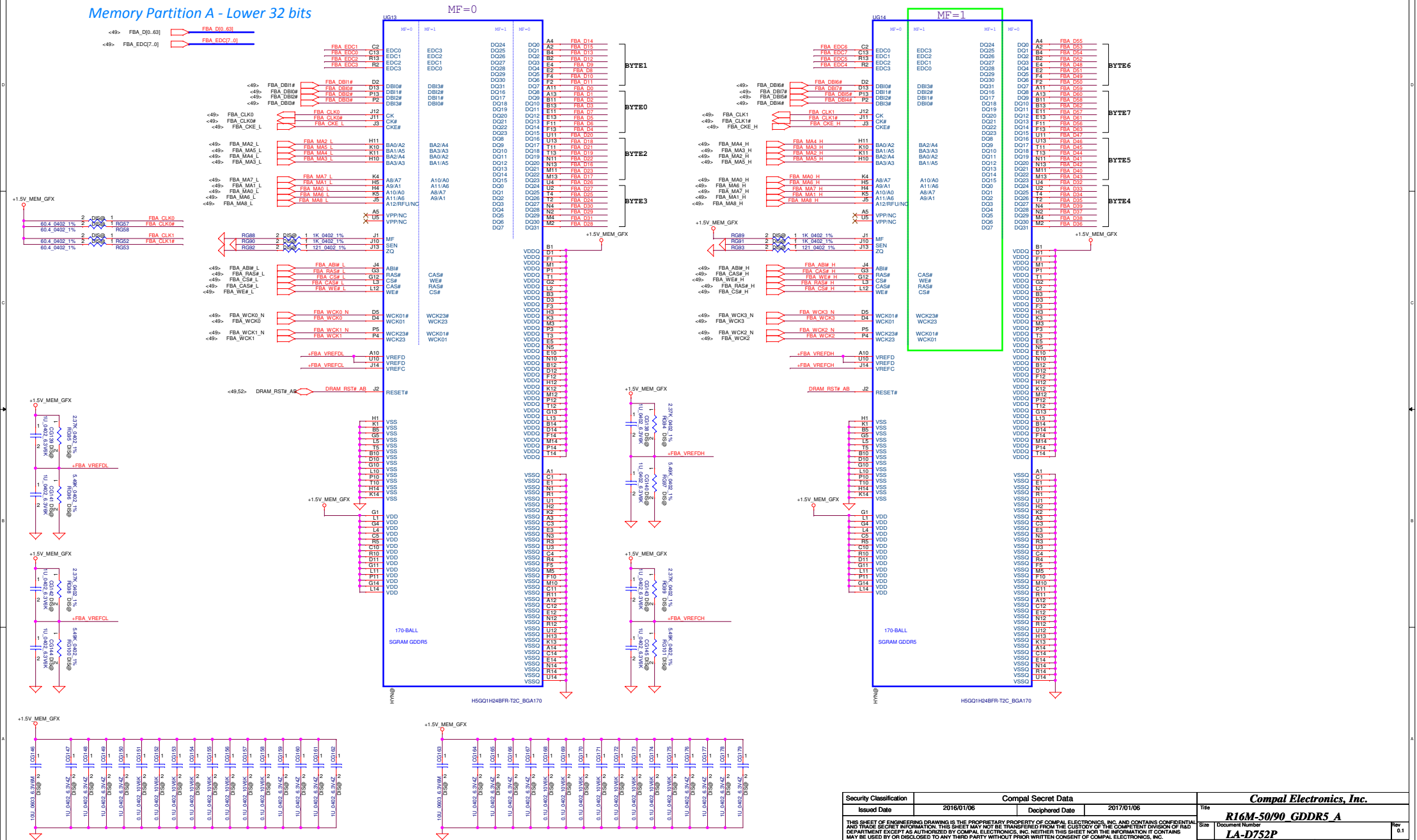
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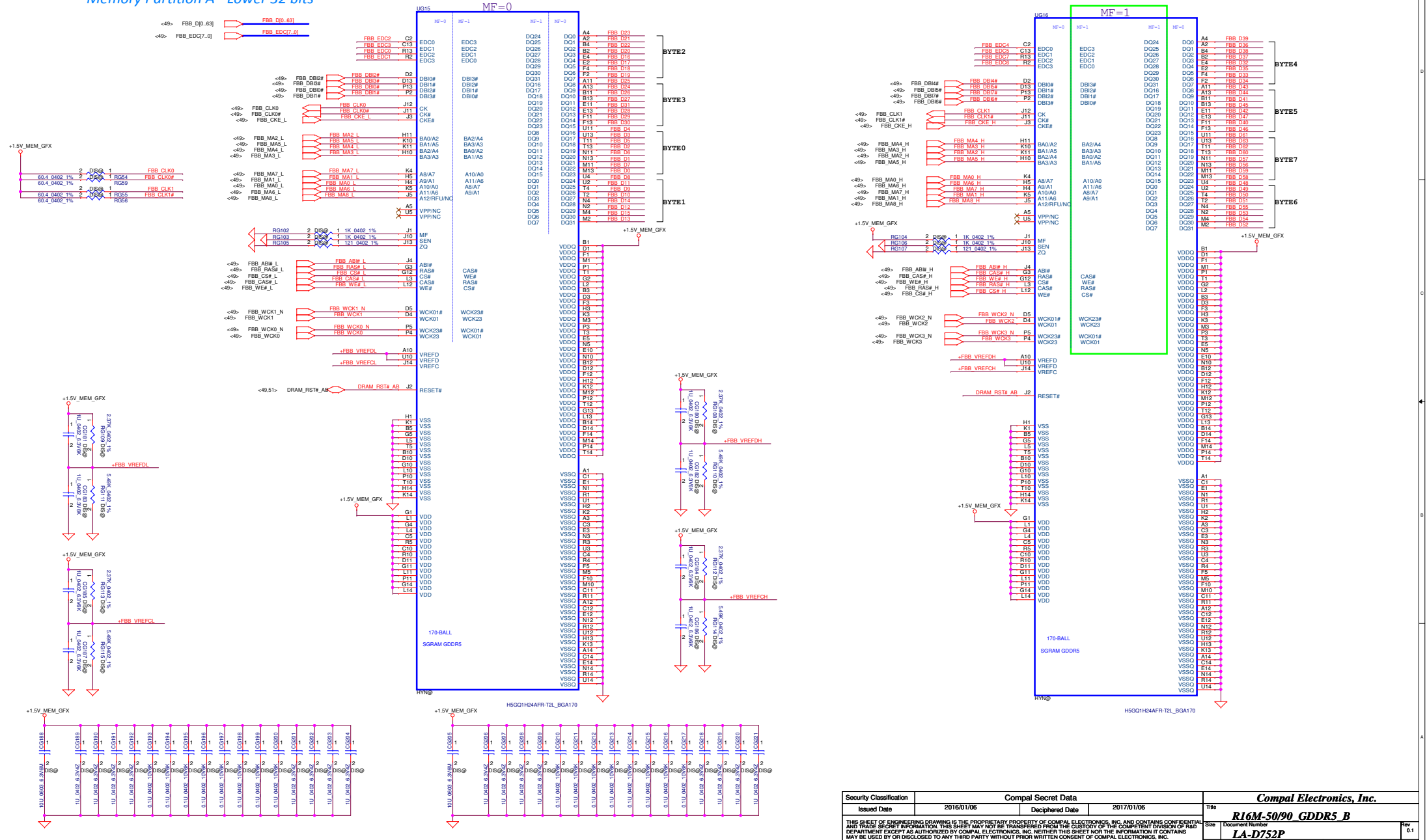


Memory Partition A - Lower 32 bits



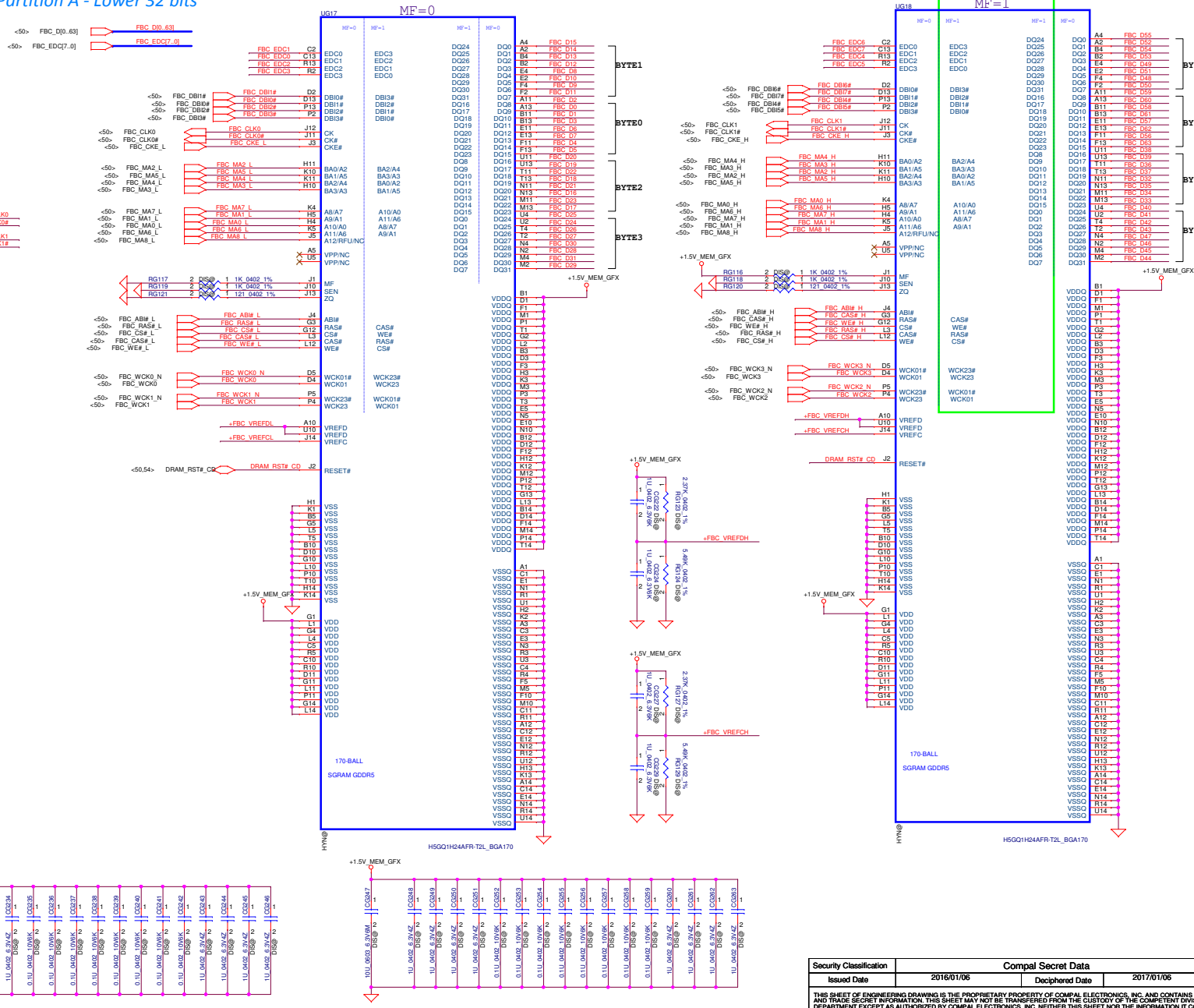
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						Date:		Thursday, January 21, 2016			Sheet

Memory Partition A - Lower 32 bits



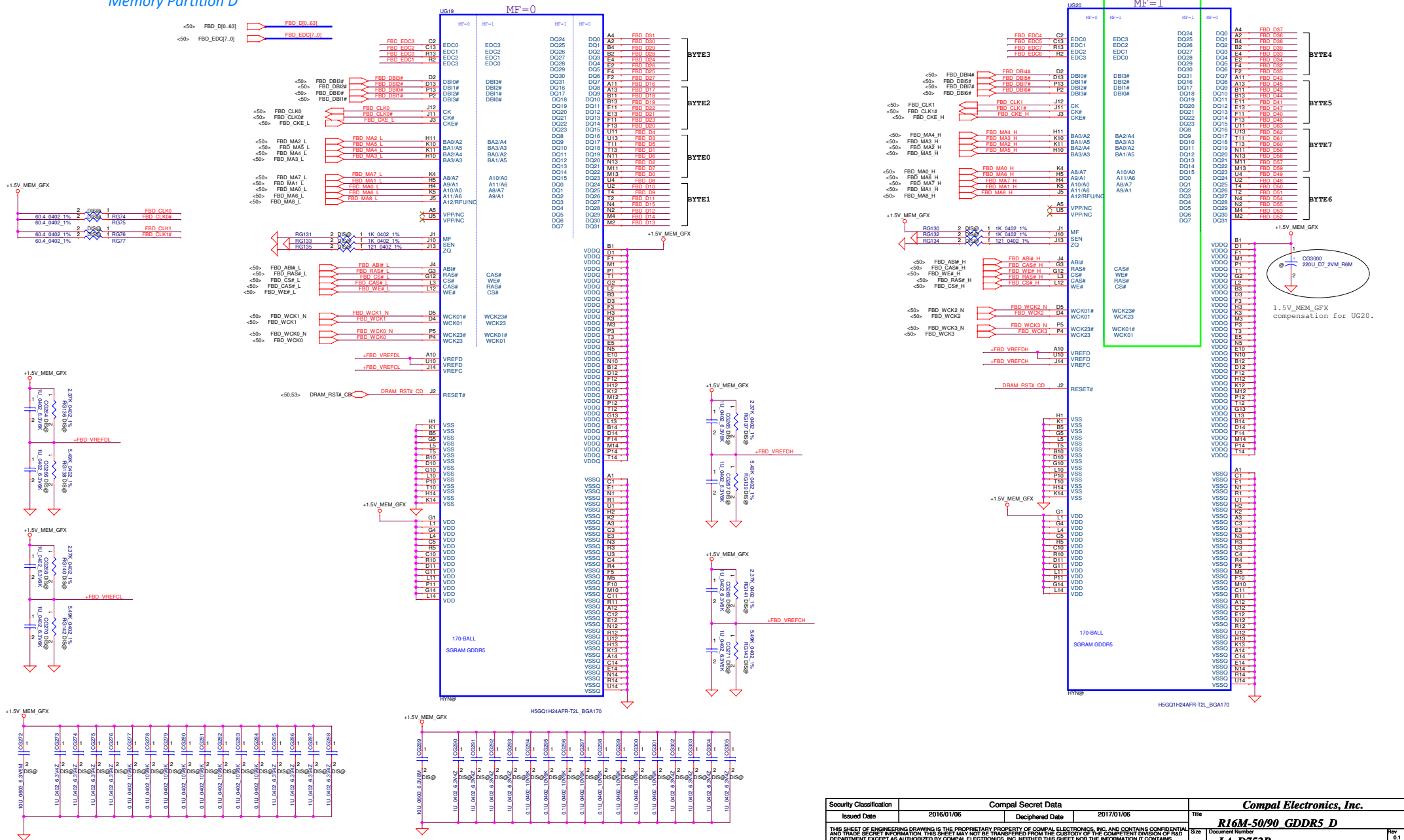
Security Classification	Compel Secret Data		<b>Compel Electronics, Inc.</b>	
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title
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				<b>R16M-50/90 GDDR5 B</b> <b>LA-D752P</b>
				Rev 0.1

Memory Partition A - Lower 32 bits



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Date: Thursday, January 21, 2016			Sheet 53 of 82	

### Memory Partition D



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Date			January 21, 2016	Sheet 54 of 82

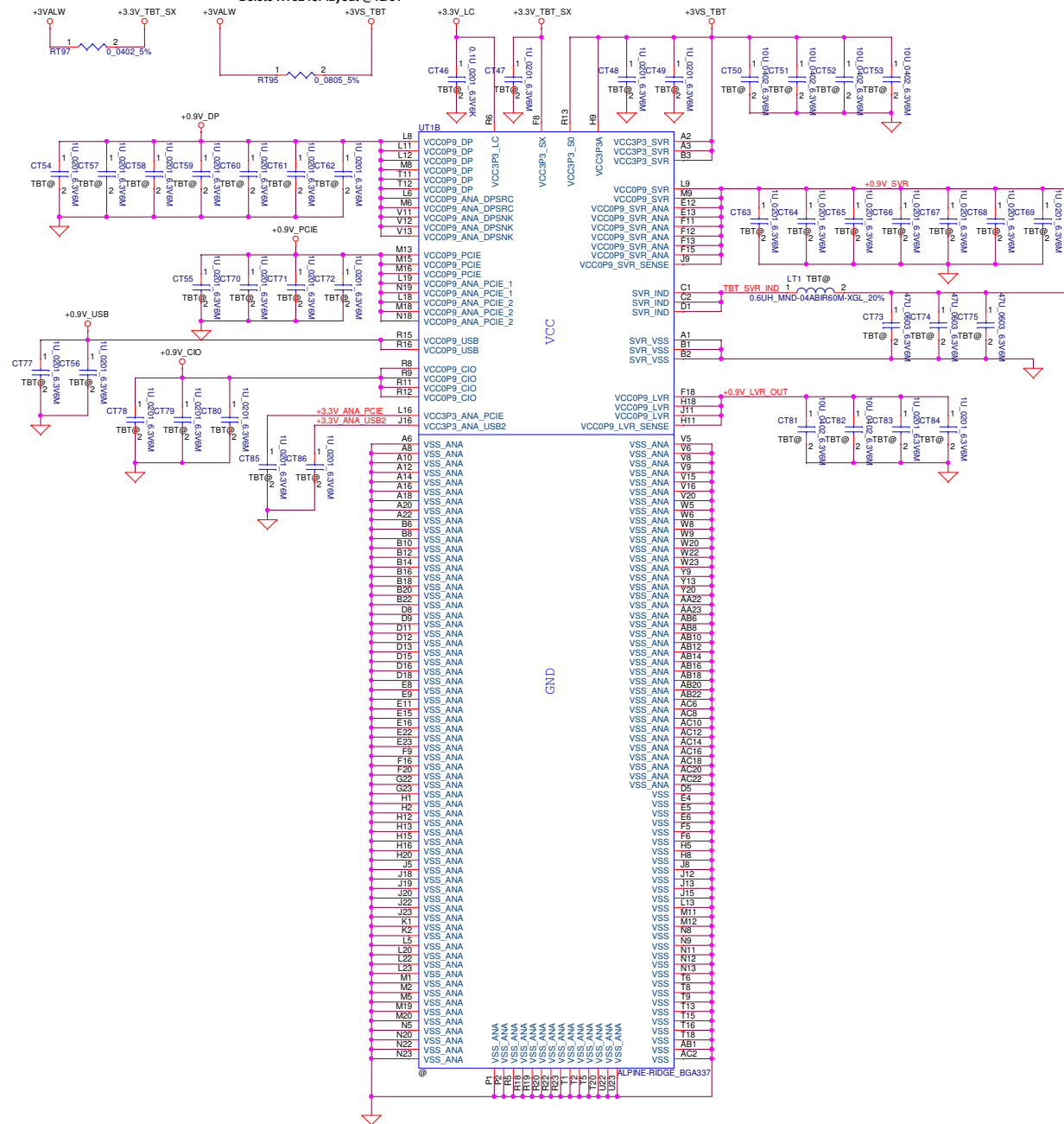


AMD GPIO Strapping <sup>1</sup>	Setting <sup>2</sup>	Name <sup>3</sup>	Description <sup>4</sup>
GPIO 29 <sup>5</sup>	Pull low 10K ohm <sup>6</sup>	BIF_VGA_DIS <sup>7</sup>	0: VGA Controller capacity enabled. <sup>8</sup> 1: The device will not be recognized as the system's VGA controller (for <sup>9</sup> headless designs). <sup>10</sup>
GPIO 20 <sup>5</sup>	Pull up 10K ohm <sup>6</sup>	TX_DEEMPH_EN <sup>7</sup>	PCI Express transmitter deemphasis enable <sup>8</sup> 0: Tx de-emphasis disabled. <sup>9</sup> 1: Tx de-emphasis enabled. <sup>10</sup>
GPIO 0 <sup>5</sup>	DNI as default <sup>6</sup>	TX_HALF_SWING <sup>7</sup>	Controls the transmitter <sup>8</sup> full/half swing mode. <sup>9</sup> 0: The transmitter full swing is enabled. <sup>10</sup> 1: The transmitter half swing is enabled. <sup>11</sup>
GPIO 22 <sup>5</sup>	Pull low 10K ohm <sup>6</sup>	BIOS_ROM_EN <sup>7</sup>	Enable external BIOS ROM device. <sup>8</sup> 0: Disable external BIOS ROM device. <sup>9</sup> 1: Enable external BIOS ROM device. <sup>10</sup>
GPIO 11 <sup>5</sup>	Pull up 10K ohm <sup>6</sup>	ROM_CONFIG[2:0] <sup>7</sup>	If BIOS_ROM_EN = 0, then ROM_CONFIG[2:0] defines the primary memory aperture size. <sup>8</sup> GPIO_[13:12:11]=001=256MB. <sup>9</sup>
GPIO 12 <sup>5</sup>	Pull low 10K ohm <sup>6</sup>		
GPIO 13 <sup>5</sup>	Pull low 10K ohm <sup>6</sup>		
Hsync <sup>5</sup>	NC <sup>6</sup>	Reserve <sup>7</sup>	Reserve <sup>8</sup>
Vsync <sup>5</sup>	NC <sup>6</sup>		
DBGDATA2 <sup>5</sup>	Pull up 10K ohm <sup>6</sup>	AUD_PORT_CONN <sup>7</sup> [2:0] <sup>8</sup>	Determine the maximum number of digital display audio endpoints. <sup>9</sup> 101: Two usable endpoints. <sup>10</sup>
DBGDATA1 <sup>5</sup>	Pull low 10K ohm <sup>6</sup>		
DBGDATA0 <sup>5</sup>	Pull up 10K ohm <sup>6</sup>		
GPIO 1 <sup>5</sup>	Pull up 10K ohm <sup>6</sup>	SMBUS_ADDR <sup>7</sup>	Provide a strap option to change the SMBUS slave address of the GPU. <sup>8</sup> 0: 0x40 <sup>9</sup> 1: 0x41 <sup>10</sup>
GPIO 2 <sup>5</sup>	Pull up 10K ohm <sup>6</sup>	BIF_GEN3_EN_A <sup>7</sup>	PCIe Gen3 capability. <sup>8</sup> 1: PCIe Gen3 is supported. <sup>9</sup> 0: PCIe Gen3 is not supported. <sup>10</sup>
GPIO 8 <sup>5</sup>	connect CLKREQ#_GPU and add pull up. DNI as default. <sup>6</sup>	BIF_CLK_PM_EN <sup>7</sup> (Reserve) <sup>8</sup>	Determines whether or not the PCIe reference clock power management <sup>9</sup> capability is reported in the PCI configuration space (otherwise known as CLKREQB). <sup>10</sup> 0: The CLKREQB power management capability is disabled. <sup>11</sup> 1: The CLKREQB power management capability is enabled. <sup>12</sup>
WAKEB <sup>5</sup>	Pull low 10K ohm <sup>6</sup>	OBFF <sup>7</sup>	0: Disable. <sup>8</sup>
SVI2_SVC <sup>5</sup>	Pull up 1Kohm <sup>6</sup>	Boot up voltage <sup>7</sup>	SVC:SVD=[1:0]=0.90V <sup>8</sup>
SVI2_SVD <sup>5</sup>	Pull low 1K ohm <sup>6</sup>		

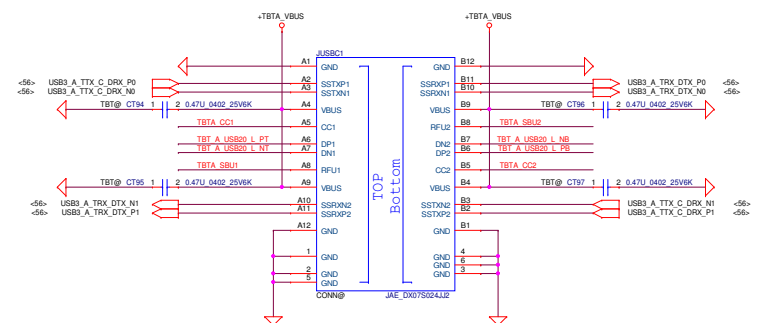
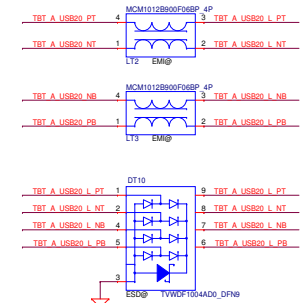
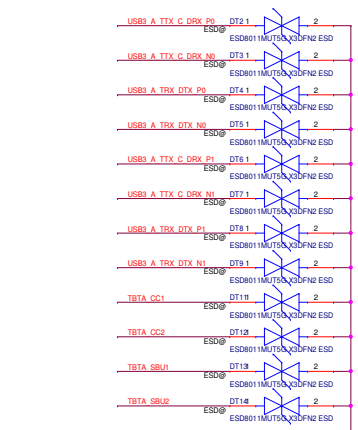




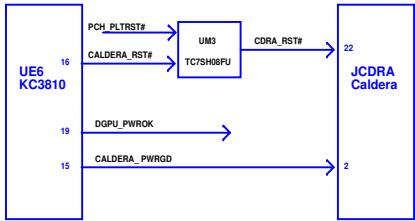
Delete RT104 for layout @12/31



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Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title	
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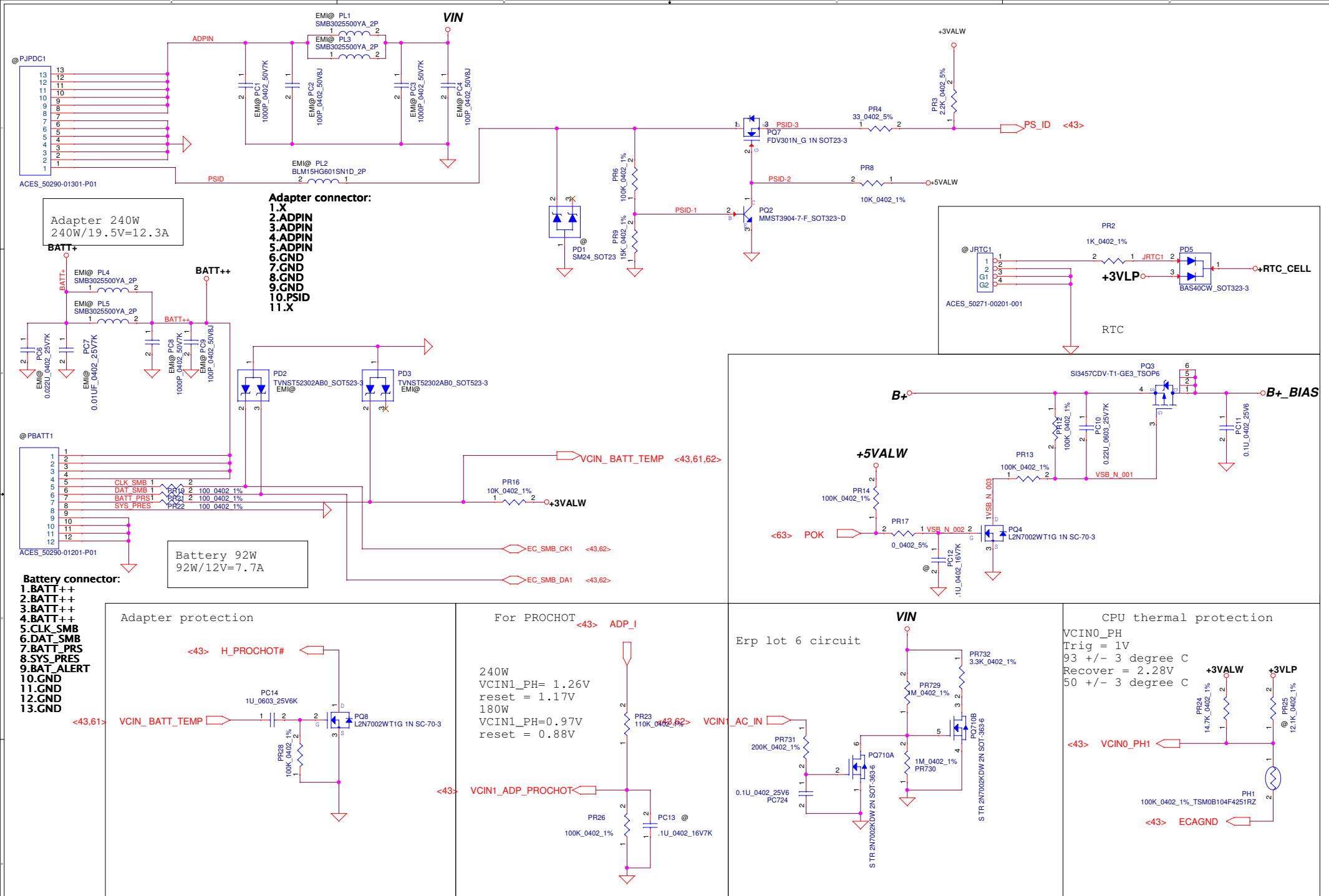


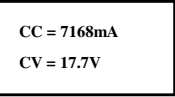
Security Classification	Compel Secret Data		Title		<b>Compel Electronics, Inc.</b>	
Issued Date	2016/01/06	Deciphered Date	2017/01/06	<b>PD-USB3.1 type C</b> <b>LA-D752P</b>		
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				Date:	2017/01/21, 2016	Sheet 58 of 80



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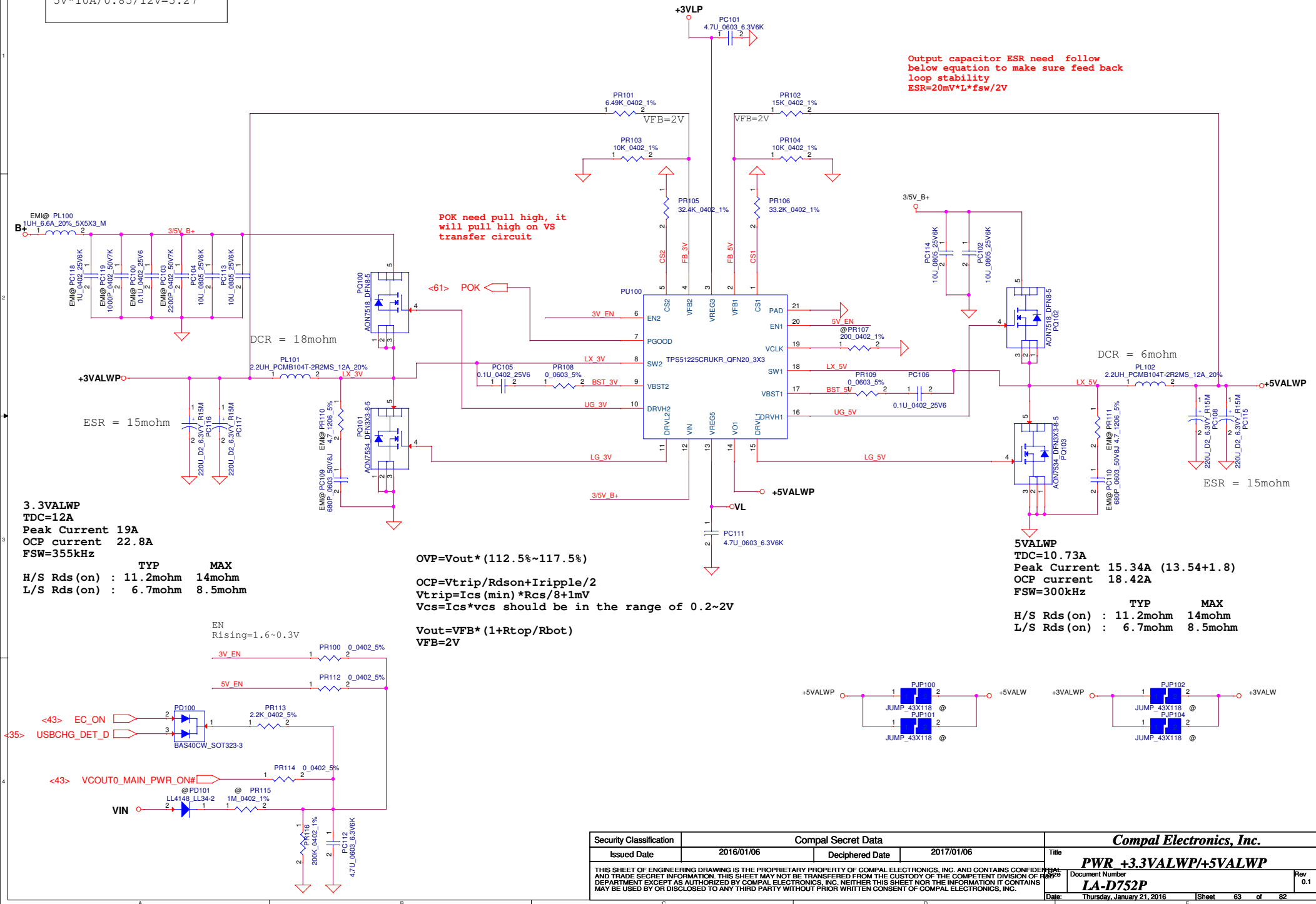




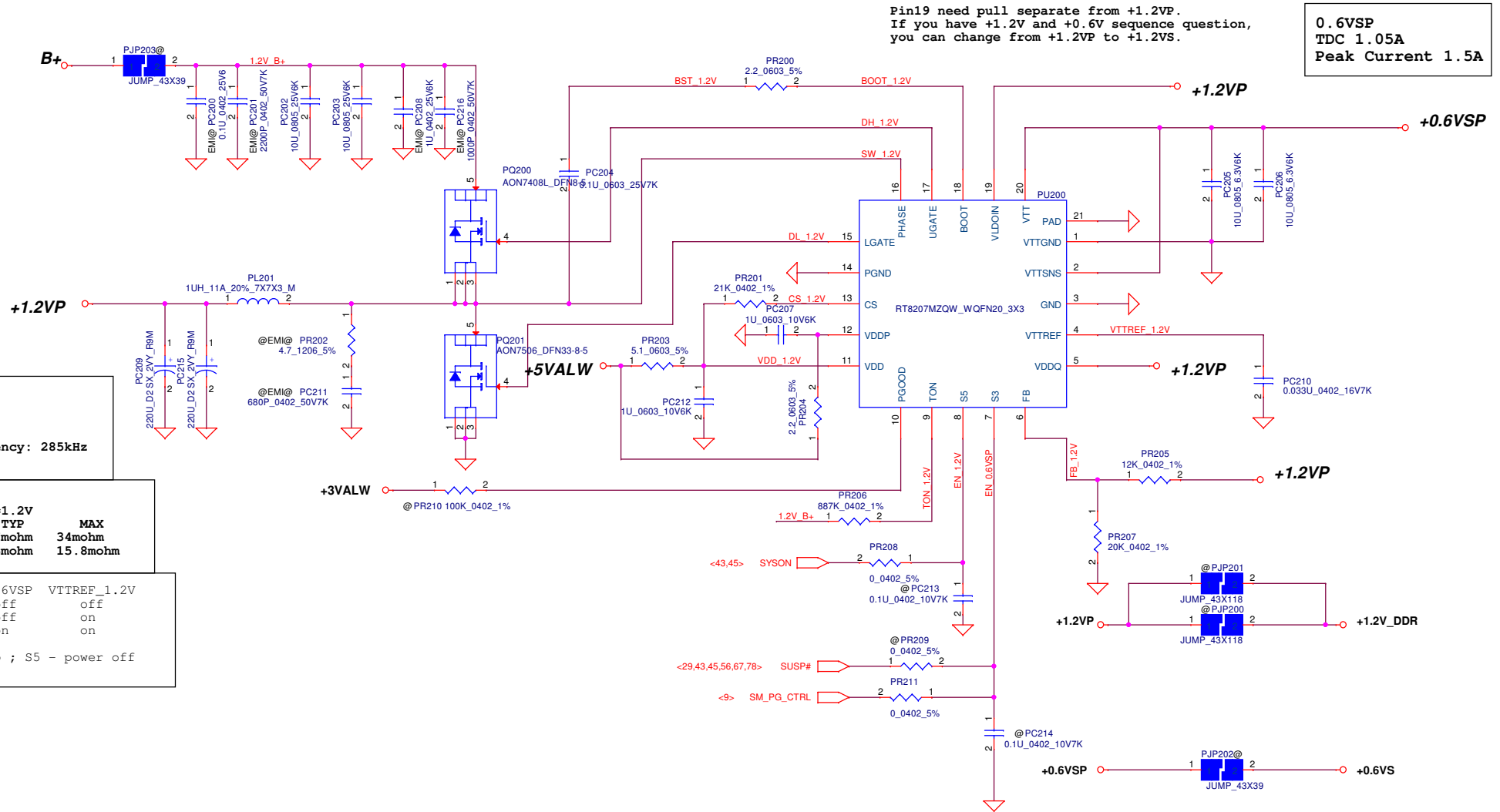
Adapter = 180W  
 $CP = 180W/19.5V \times 0.9 = 8.30A$   
 $APDI = 1.66V$   
 $Hybrid\ trigger = CP \times 107\% = 8.88A$   
 $ADPI = 1.77V$   
 $IPCC = 180W/19.5V \times (1 \times 0.95) = 8.77A$   
 $ADPI = 1.75V$   
 $IPCC(hybrid\ mode) = 180W/19.5V = 9.23A$   
 $ADPI = 1.85V$   
 $PROCHOT = 180W/19.5V + 1 = 10.23A$   
 $ADPI = 2.04V$

Security Classification	Compal Secret Data			Title	
Issued Date	2016/01/06	Deciphered Date	2017/01/06	PWR CHARGER	
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Input Current: 7.5A  
 $3.3V \times 10A / 0.85 / 12V = 2.23$   
 $5V \times 10A / 0.85 / 12V = 5.27$



$$\text{Input Current: } 1\text{A} \\ 1.2\text{V} \times 8.88\text{A} / 0.85 / 12\text{V} = 1$$



1.2VP  
TDC=9A  
Ipeak=12.86A  
OCP=15.43A  
Switching Frequency: 285kHz

OVP: 110%~120%	
VFB=0.75V, Vout=1.2V	
TYP	MAX
H/S Rds(on) : 27mohm	34mohm
L/S Rds(on) : 13mohm	15.8mohm

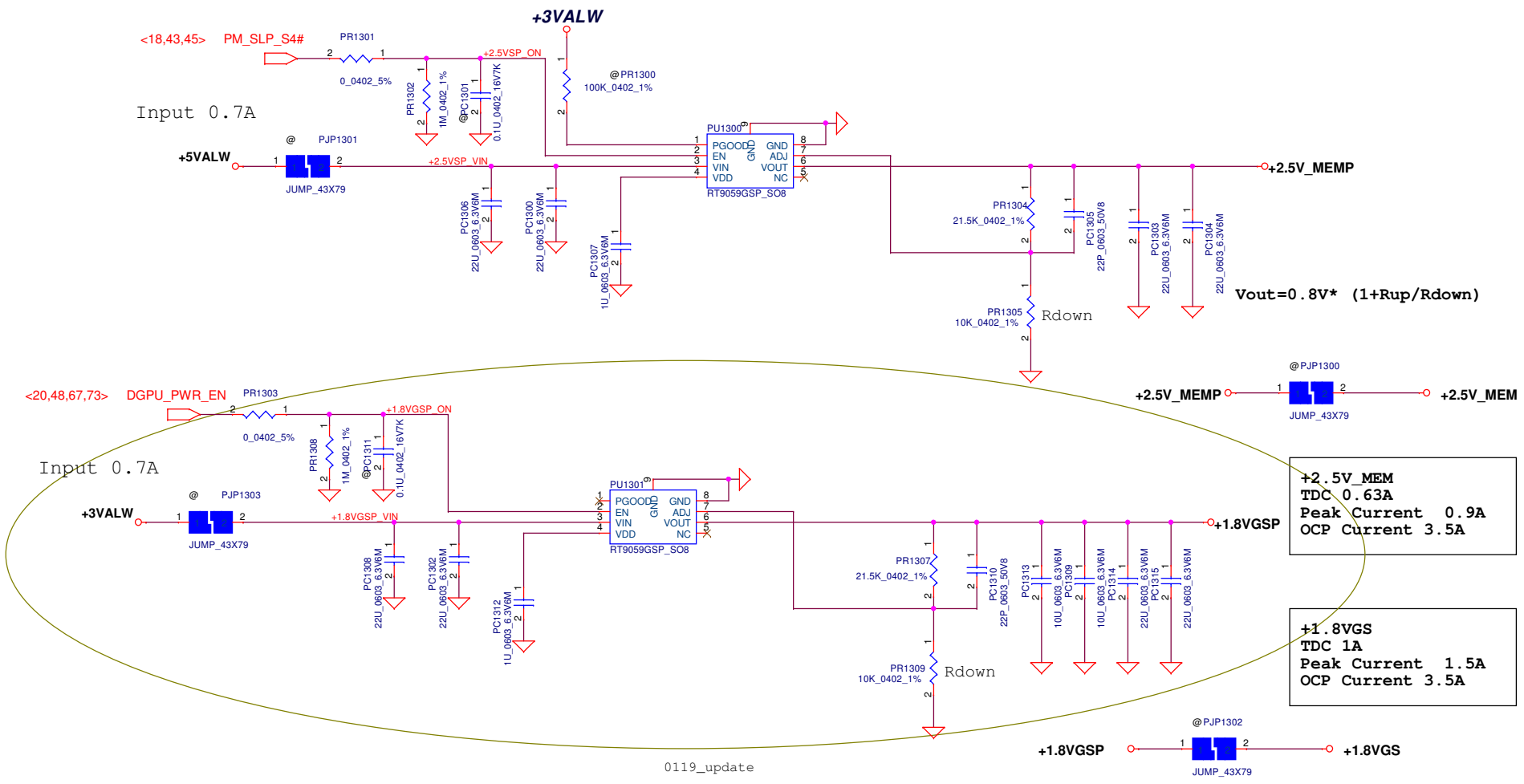
Mode	Level	+0.6VSP	VTTREF_1.2V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Note: S3 - sleep ; S5 - power off

Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>PWR +1.2V/+0.6VSP</b>	
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title	
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				<b>LA-D752P</b>	
				Date:	Thursday, January 21, 2016
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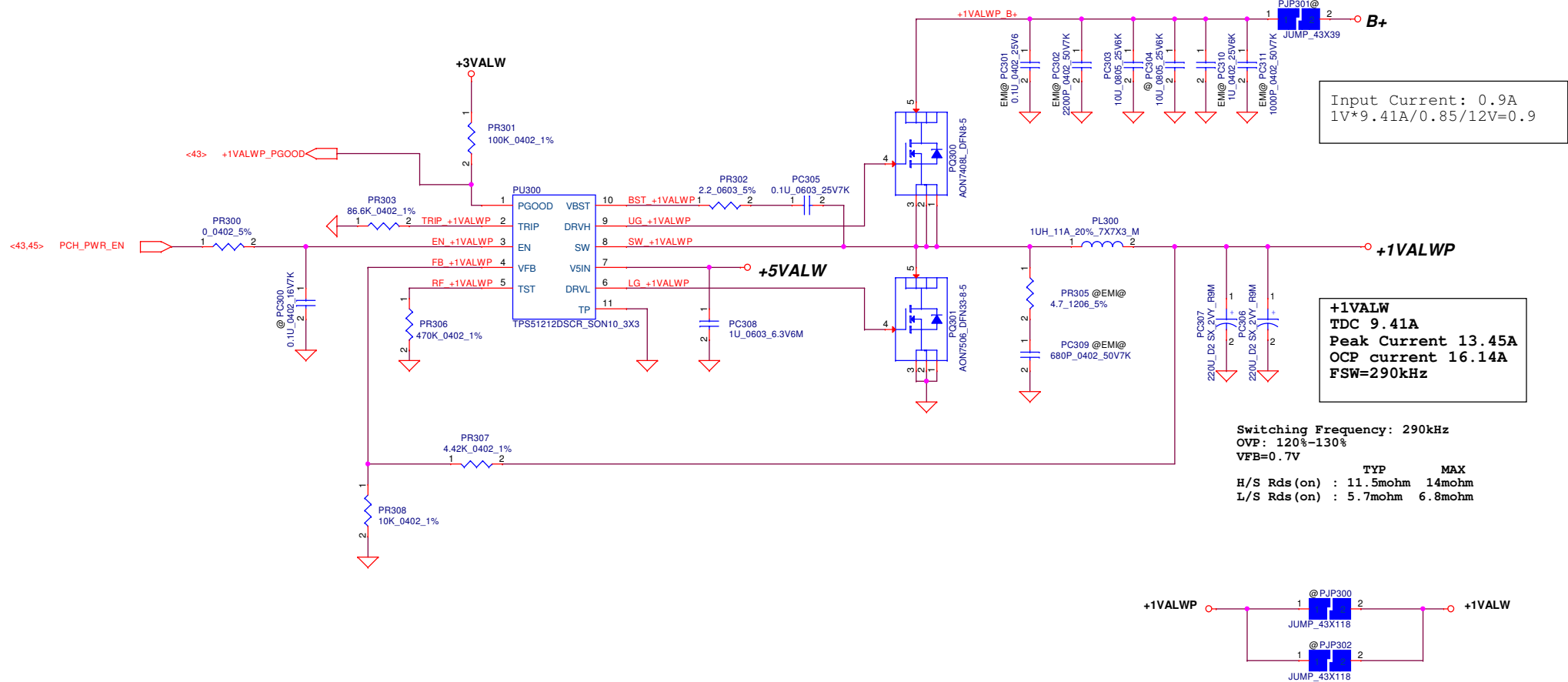




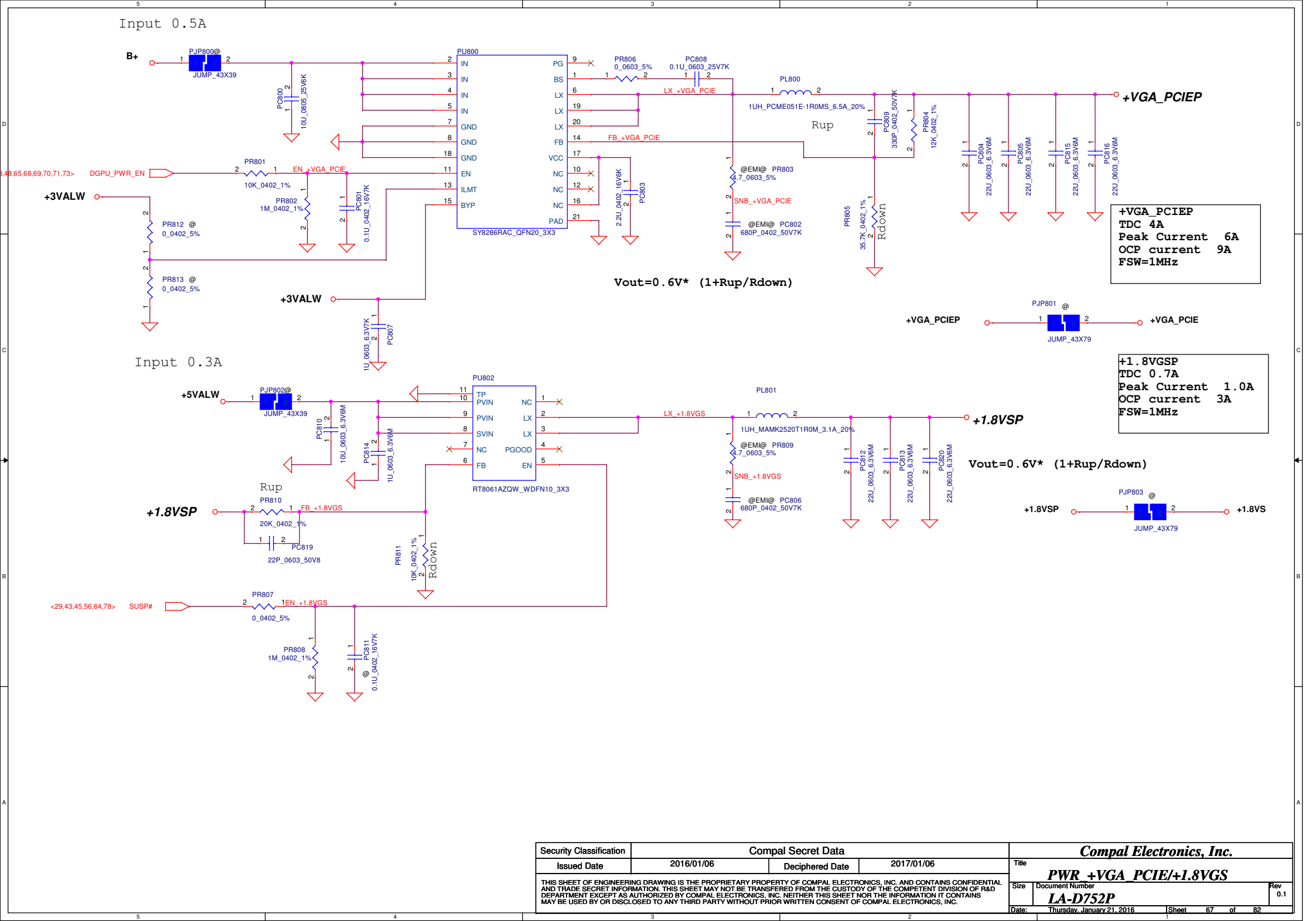
**+2.5V\_MEM**  
TDC 0.63A  
Peak Current 0.9A  
OCP Current 3.5A

**+1.8VGS**  
TDC 1A  
Peak Current 1.5A  
OCP Current 3.5A

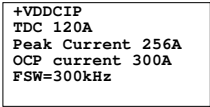
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title	<b>PWR +2.5V MEM/+1.8VGS</b>
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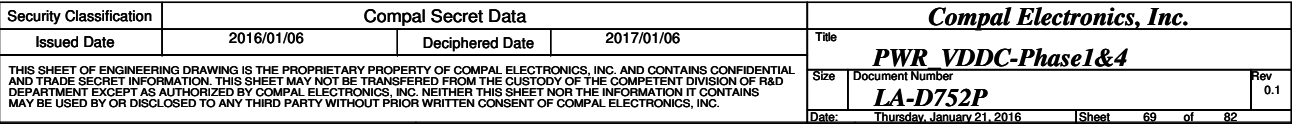
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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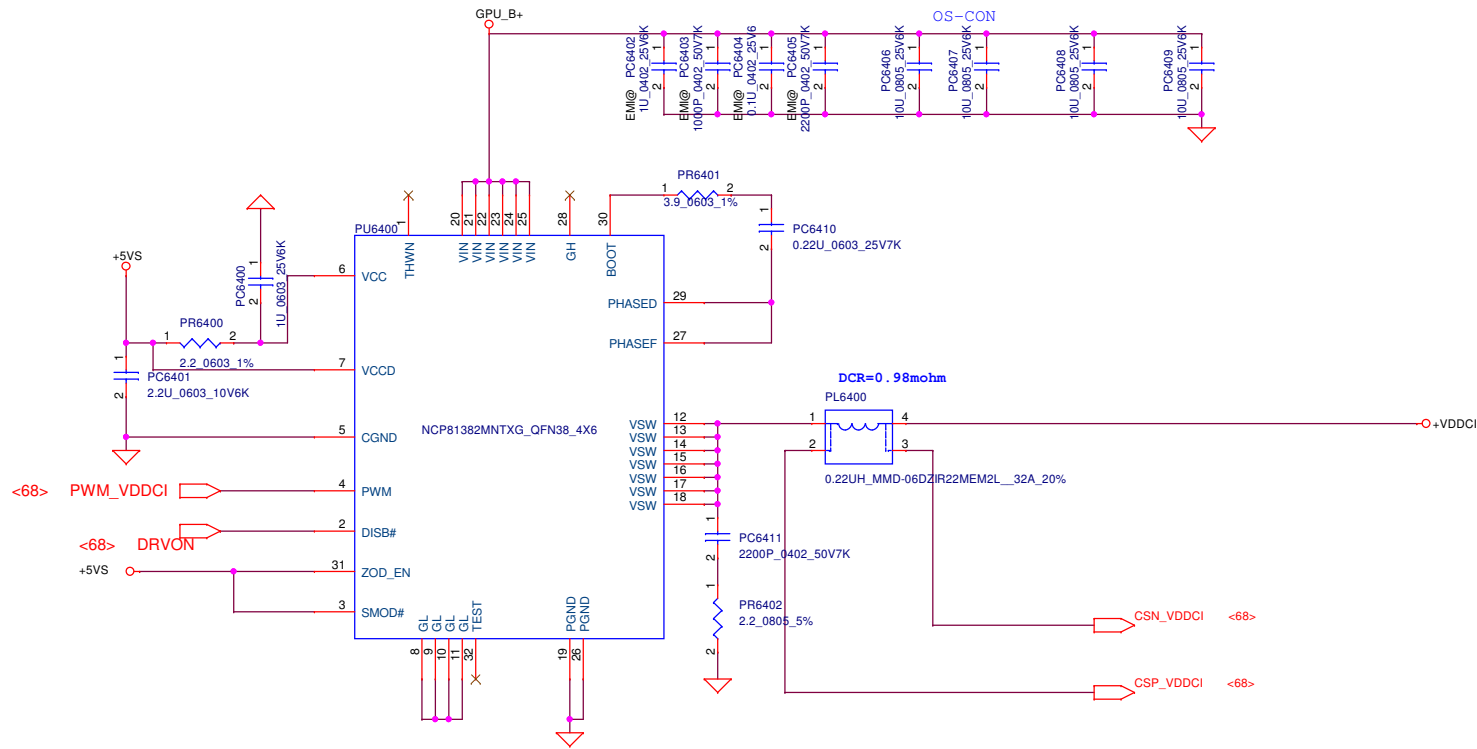


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Size	10.00	Sheet	9016	Rev 0.1
		Columns	68	of 93









Input Current: 0.7A  
 $1V \times 7A / 0.85 / 12V = 0.9$

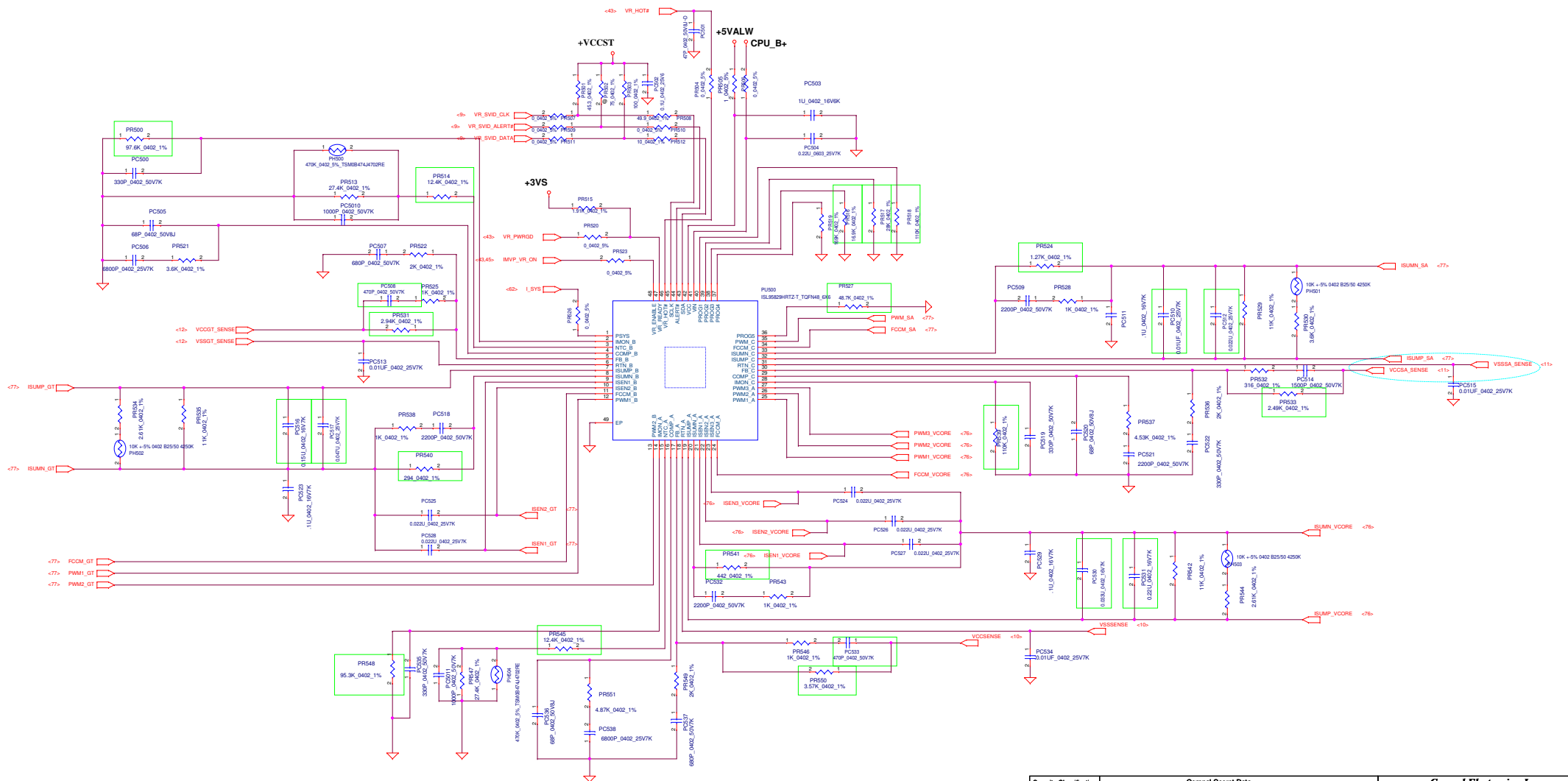
**+VDDCIP**  
**TDC 10A**  
**Peak Current 15A**  
**OCF current 20A**  
**FSW=600kHz**

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Size	Document Number	Rev		0.1	
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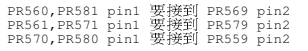






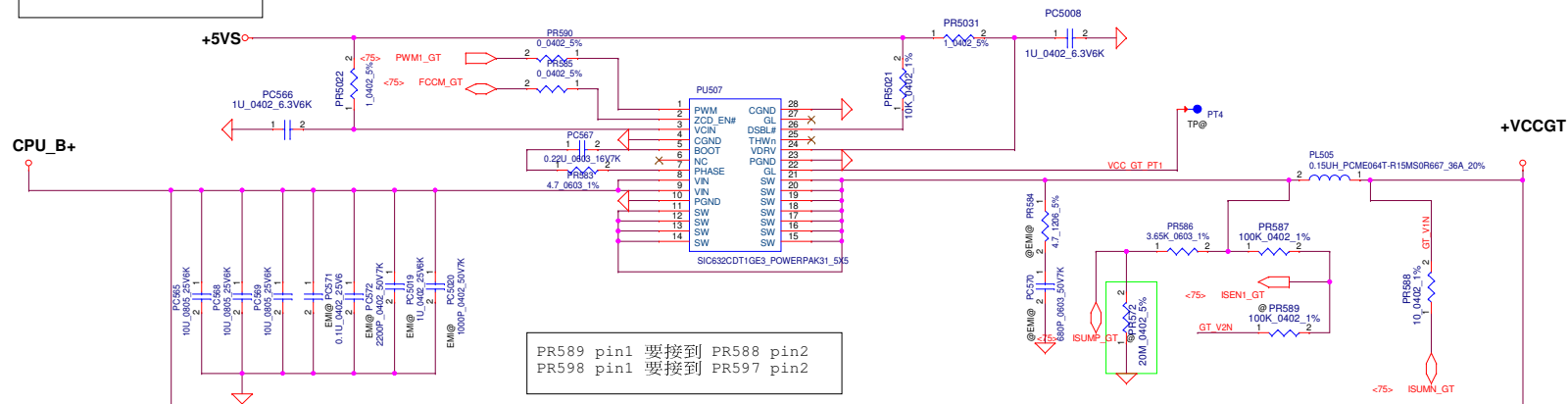
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2016/01/08	Disseigned Date	2017/01/08	File	PWR_VCORE ISL95855
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VCC\_CORE  
TDC\_PL2 :56A  
Peak Current 68A  
OCP Current 81.6A  
DCR 0.66mohm +/-7%  
Load Line 1.8mV/A

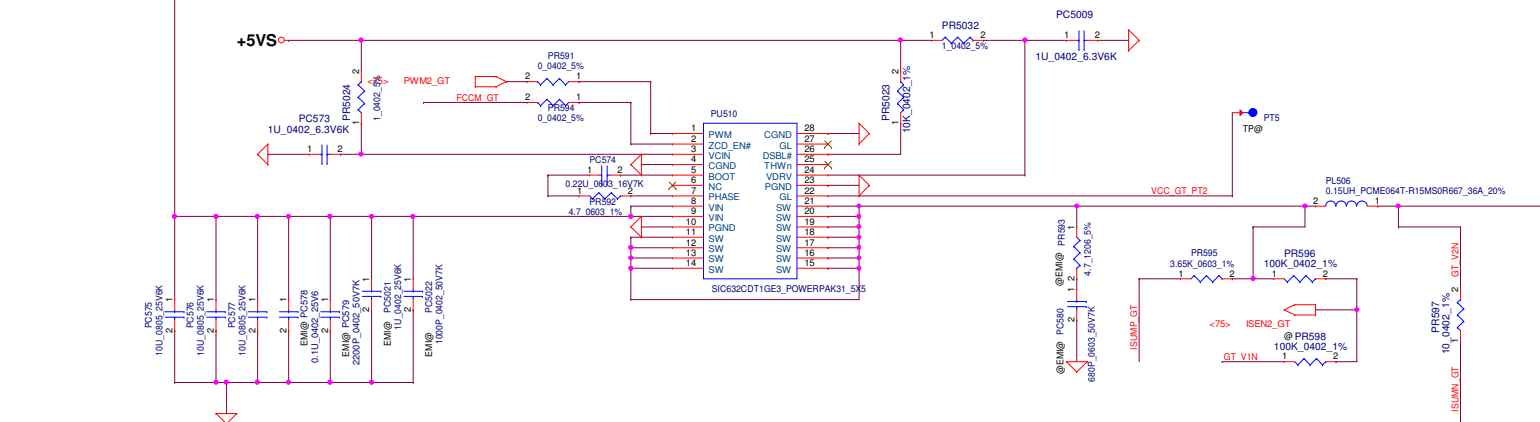


Security Classification	Compul Secret Data		Title		<b>Compul Electronics, Inc.</b>	
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Doc Number		<b>PWR VCORE +VCC CORE</b>
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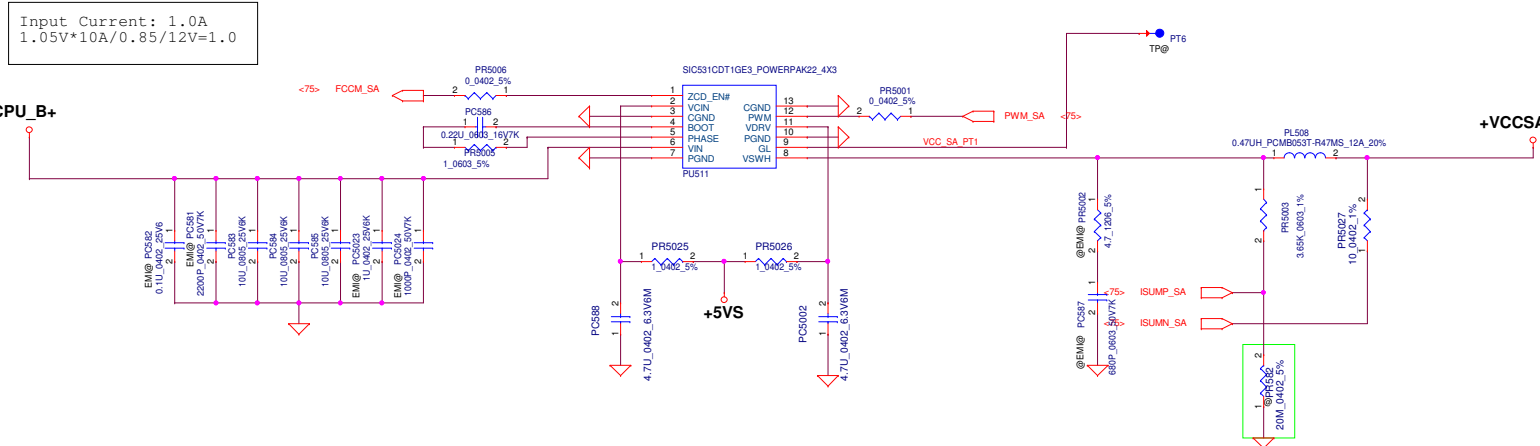
Input Current: 5.7A  
 $1.5V \times 39A / 0.85 / 12V = 5.7$



VCC\_GT  
TDC PL2 : 39A  
Peak Current 54A  
OCP Current 64.8A  
DCR 0.66mohm +/-7%  
Load Line 2.65mV/A



VCC\_SA  
TDC PL2 : 10A  
Peak Current 11A  
OCP Current 13.2A  
DCR 7.4mohm typ  
Load Line 9.1mV/A





+VCC\_CORE

+VCCGT

+VCCSA

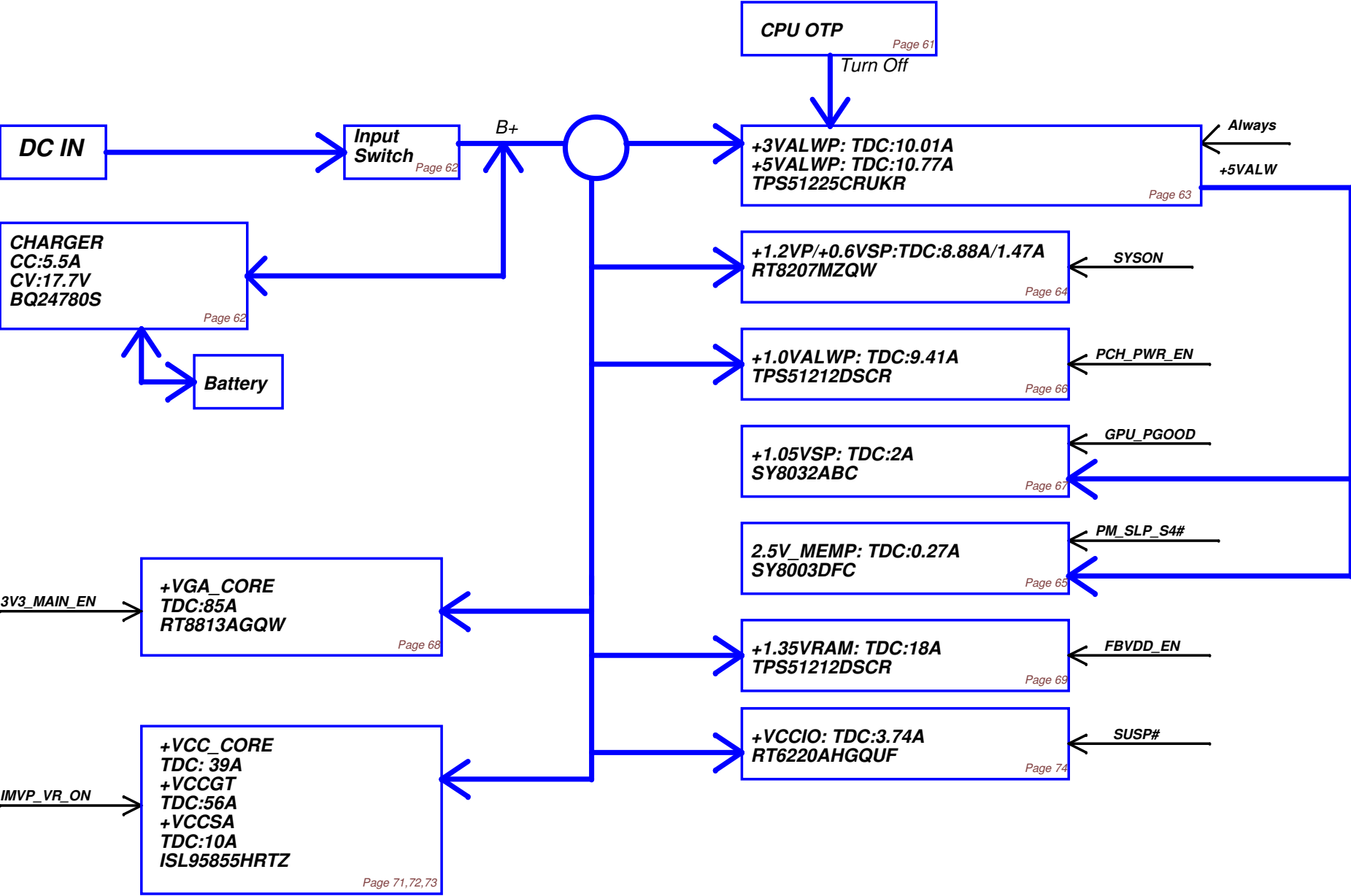
VCC\_CORE  
220uF X3  
47uF\_0805 X 4  
22uF\_0603 X 8  
10uF\_0402 X 28  
1uF\_0201 X 63

VCC\_GT  
220uF X4  
47uF\_0805 X 6  
22uF\_0603 X 8  
10uF\_0402 X 35  
1uF\_0201 X 68

VCC\_SA  
220uF X1  
47uF\_0805 X 1  
10uF\_0402 X 7  
1uF\_0201 X 3

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Power block





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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
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